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C—3—2 Electrical Characterization of Micro Defects in Silicon Crystal

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Various defects, such as the oxide precipitates(OP's), the dislocation loops (DL's) and the stacking faults(SF's) were introduced into the wafers by the two-step annealing.[1] Role of such micro defects in silicon as the carrier recombination centers has been investigated.

CZ boron-doped <100> silicon crystal ingot(resistivity: 11~8 ohm·cm, oxygen content: 12.3~8 x10^{17} cm^{-3}) was sliced into wafers. The annealing conditions were chosen to control the defect kind and density, and are listed in Table 1. The first annealing was carried out in an argon atmosphere for 180 minutes. The second annealing(oxidation in dry O_2) was carried out at several temperatures forming almost the same SiO_2 thickness(1500 Å). After H_2 treatment, bulk lifetime τ , by the photo-conductivity decay method, was measured on each wafer. Then, the wafers were etched to thin films to observe the defects with transmission electron microscope(TEM).

Distributions of τ and the bulk stacking fault density SFD along the ingot axis are shown in Figure 1. Lifetime in Figure 1 is classified into three groups (A), (B) and (C). There existed SF's(0.3~7 μm dia.) in each wafer, and high density DL's(0.1~0.3 μm dia.) and OP's(0.05~0.3 μm dia.) in the gruops (B) and (C). Typical defect densities of the gruops are listed in Table 2. Microphotographs in Figure 2 are typical TEM images of these gruop wafers from near the ingot top. The relation between τ and SFD(included various SF dia.) is plotted in Figure 3 (a). Note that τ is proportionally decreased by SFD and expressed as $1/\tau \propto (SFD)^{1/3}$ at the region of SFD $> 10^4$ cm^{-3}. The index 1/3 is different from that obtained by MOS C-t measurement[2),3)](0.7~1). The reason for this discrepancy is considered that τ is influenced by the carrier diffusion process. Comparing (A) with (B) in Figure 1 and Table 2, it is found that DL's and OP's also have electrical activity. Figure 3(b) shows the relation between τ and total defect density for 0.3, 3 and 7 μm defect diameter. In this case, lifetime depends on defect density and size, so that apparent SF activity in Figure 3(a) is influenced by total defect density and size. On the other hand, lifetime in the depletion region depends only on defect density.[2)] Annealing T_3 was found to generate high density OP's, DL's and SF's to result in very low τ values.

In summary, it has been shown that not only the stacking faults, but the dislocation loops and the oxide precipitates have electrical activity, and they decrease bulk lifetime by the index of 1/3.

References:

1) H. Takaoka, J. Oosaka and N. Inoue, Japan. J. appl. Phys., 18(1979) Suppl. 18-1, 179.
2) Y. Matsuoka, K. Ikuta and S. Nakajima, Japan. J. appl. Phys., 17(1978) 2167.
3) H. Strack, K. R. Mayer and B. O. Kolbesen, Solid-State Electronics, 22(1979) 135.

Table 1. Annealing conditions.

	first		second	
	temp.(°C)	time(min)	temp.(°C)	time(min)
T_1	—	—	1050	120
T_2	650	180	1050	120
T_3	750	180	950	380
T_4	850	180	1200	30
T_5	950	180	1050	120
T_6	750+1050	180+180	1050	120

Table 2. Defect densities in cm^{-3}.

group	τ	SFD	DLD	OPD
A (T_2)	high	$2x10^6$	ND	ND
B (T_5)	middle	$4x10^6$	$1x10^8$	$3x10^9$
C (T_3)	low	$5x10^9$	$2x10^{11}$	$8x10^{11}$

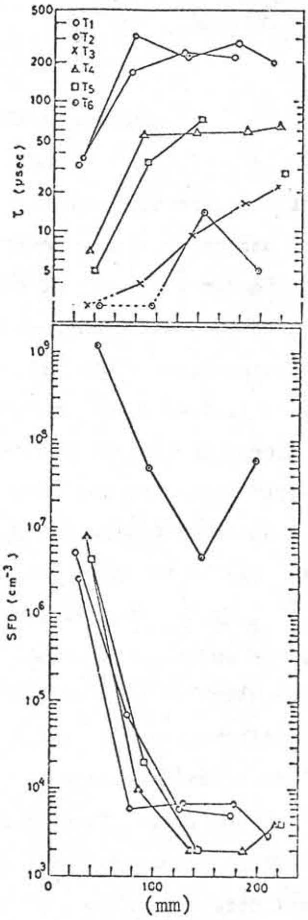
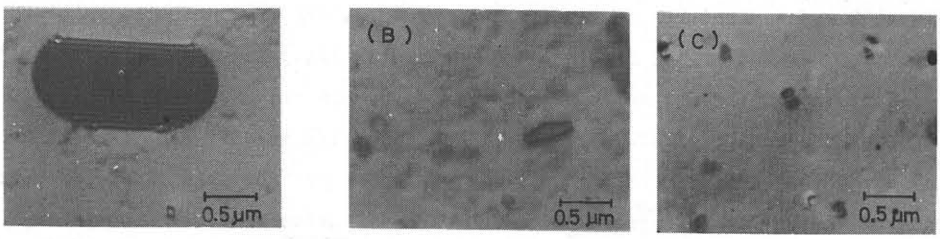
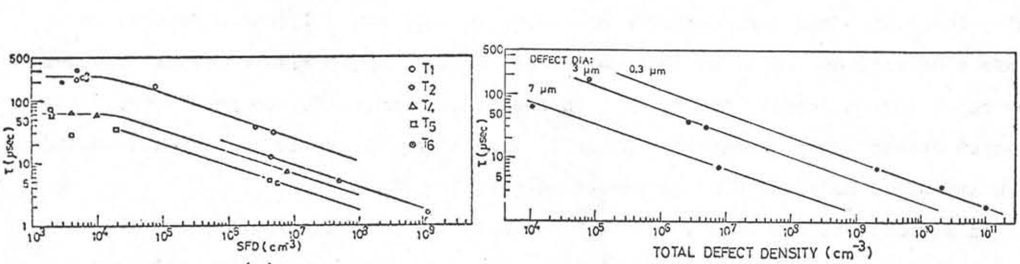


Fig. 1. Distributions of SFD and τ along the crystal axis.



(a) A stacking fault. (b) DL's and OP's.

Fig. 2. Microphotographs of defects.



(a) (b)

Fig. 3. Relations between τ and defect density.