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MOSFET DEVELOPMENT IN IBM - 1963 TO PRESENT

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In 1963, IBM's Research Division started a comprehensive MOSFET program aimed toward Large Scale Integration(LSI) of logic. An early decision was made to pursue the more difficult n- channel technology rather than p- channel based on the 3x higher mobility and evaluations of power/performance requirements. This was contrary to the main thrust of the industry. Several advances in the 1960's were key to the success of the n- channel technology in IBM including: a) the development of PSG gate oxide passivation techniques(1) which dramatically decreased Na contamination problems and increased yield and reliability, b) the development of annealing techniques to enhance mobility and to reduce surface and insulator charge and c) the realization that the use of a negative substrate bias on the silicon substrate could be used to "turn-off" the n- channel device, reduce surface leakage problems and improve the overall device/circuit design(2).

In early 1966, the Research Division launched an aggressive advanced development program to develop MOSFET memory to replace ferrite cores. This led to a joint development program with the product divisions in 1967-68. The performance advantage of the bipolar technology was capitalized on by the use of bipolar support chips for higher level decode functions, off-chip sense amplifiers and high current drivers(3). The decision was made in January 1968, that IBM would use integrated circuit memory including both bipolar and MOSFET rather than ferrites in all future main memory product development. The first bipolar(128 bit chip) semiconductor main memory was shipped in the System/370 Model 145 in 1971.

The MOSFET development work resulted in a working 512-bit chips in 1968, the shipment of engineering parts to systems developers in 1970, the introduction to large scale manufacturing in 1971 of a metal gate process with a 70 nm gate insulator and shipment in large systems (the System/370 Model 158) in 1972. The first product had 1024 bits/chip with a typical chip access time of 50 ns. Quartz passivation and the flip chip joining technology allowed four chips to be packaged on a multichip module. This was followed shortly by a 2048 bit/chip design with 8K bits/module(4). The modules were packaged on organic cards and boards to form a 2M byte system. To meet reliability and serviceability requirements, severe specifications were put on component reliability and ECC was used at the system level.

The same technology was used to develop and manufacture logic, ROS, RAM and PLA chips for applications in smaller machines. In order to handle the large number(many 100s) of designs - systems for chip design, test generation, manufacturing control, and release systems were developed in the early 1960's to allow IBM design engineers throughout the world to utilize the technology.

The main thrust in IBM for the second generation of RAM products, which started in several laboratories in 1970, was to take advantage of the density potential of the one-transistor cell(5). Based on considerations of complexity, density, reliability, and cost/performance trade-off's at the system level, IBM made the decision to develop a metal-gate electrode technology. A nitride-oxide gate insulator (45 nm equivalent) for enhanced gate reliability and a polysilicon field-shield to reduce surface leakage to very low levels were used. A series of products(6) including a 64K bit chip, a 32K bit chip, and a higher speed 18K bit chip were developed. The chips include redundant lines which allow bad bits or lines to be replaced after testing. Four 64K bit chips are mounted on 256K bit module with 256K bytes on a 11.4cm x 17.8cm card. The first working parts were made in 1976, production of manufacturing parts began in 1977, volume manufacturing began in 1978, and the technology was announced in October 1978 for both the System/38 and the IBM 8100.

There continue to be innovations in processes, devices and circuits. The use of low resistivity refactory metal/polysilicon conductors(7) promises to give enhanced performance. Device enhancements such as the Lightly Doped Drain(LDD) device(8) may allow higher speed circuits with shorter source-drain spacings. A continuing large leverage item is that of moving to smaller dimensions and tolerances with a "scaling" of the technology(9). IBM has done considerable work on device design, processing, etching, and exposure techniques (including electron beam) over the past decade to learn how to capitalized on these leverages. While practical limits on some parameters such as hot electron effects(10) must be considered in advanced designs, there is clearly much more progress in terms of performance, function, and cost to be made in the 1980's.

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