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BOW AND WARPAGE OF SILICON WAFERS

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During the past ten years, the wafer diameter increased from 50 mm to over 100 mm even up to 125 mm, and 200 mm diameter wafer has been made experimentally. On the other hand, the device design rule became drastically smaller and smaller to 1 micronmeter which could realized by electron beam technique. The wafer flatness in the focal plane of electron beam delineator or optical printer is crucial for an uniform imaging in the photo- or electron beam- lithographic process. This flatness is independent of wafer diameter while bow depends on the diameter.

It is important to control the wafer curvature, concave or convex in device side, to keep chucked wafers flat in any lithographic apparatus using vacuum, electrostatic or mechanical chuck depend on each conditions. Wafer warpage after repeated high temperature LSI processes has been reported to depend on initial wafer bow.

The relation between initial wafer bow and warpage caused by thermal treatment were discussed on two papers[1), 2)]. But these papers based on a simple heat treatment of wafer and on characterization data by a few measuring methods. Real time in-process observation for warping of wafer during a heat treatment was not achieved due to the difficulty of making of long working distance observation instrument with wafer warpage pattern information.

In this paper, we discuss systematically the bow and warpage during whole the process from crystal growth to heat treatment and characterization methods and their instrumentation including above mentiond real time in-process wafer warping observation instrument with pattern information. Wafer warpage in heat treatments are calculated theoretically and it is conformed to cueing the real time in-process measurement.

In situ observation of wafer heat treatment show the wafer warpage type (concave, convex and saddle) depend on initial wafer bow types. The observed thermal strain and elastic deformation of wafer were agreed well computer simulation. This elastic deformation was changed to plastic deformation at higher temperature heat treatment above critical temperature. The residual damage on the back side of wafer influenced to plastic deformation due to generation of

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dislocation by the thermal stresses.

In summary, Table 1 shows the correlation table for wafer bow and warpage over the whole the process and counterplans for wafer bow and warpage in each unit process from this study.

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TABLE 1 CORRELATION TABLE OF WAFER BOW AND WARPAGE
AND
COUNTERPLANS FOR WAFER BOW AND WARPAGE

UNIT PROCESS	CCUNTERPLANS	REF.
CRYSTAL GROWTH	OXYGEN & CARBON CONCENTRATION : $7\text{-}10 \times 10^{17}$, 4×10^{15} UNIFORM IMPURITIES DISTRIBUTION	5)
SLICING	MONITORING AND SUITABLE DRESSING TO KEEP GOOD SLICING CONDITION USING LOW INITIAL RIM BENDING BLADE	3)
(ETCHING & LAPPING)	(CAN BE SKIPPED WHEN GOOD SLICING OBTAIN)	3)
CHAMFERING & ETCHING	USING FINE GRIT ABRASIVE ETCH OFF THE DAMAGE	4)
POLISHING	BOTH SIDE FREE POLISHING WITH LOW POLISHING PRESSURE AND HIGH ETCHING RATE SLURRY	3)
HEAT TREATMENT	DISTANCE BETWEEN WAFERS LONG, PROCESS TEMPERATURE LOW PROCESS REPEAT CYCLE SMALL, HEATING VELOCITY LOW CONCAVE DEVICE SIDE WAFER SUITABLE WAFER THICKNESS	4)