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Design Considerations for High Power GTOs

Makoto Azuma, Mamoru Kurata and Hiromichi Ohashi

Toshiba Research and Development Center

Kawasaki, Kanagawa, Japan

Gate turn-off thyristors (GTOs) have received much attention lately because of their advance over thyristors that require current interruption by commutation circuits. GTOs could well find their place in various inverter and chopper circuits, since their surge current capability far exceeds that of bipolar transistors.

There are two major requirements with respect to GTO design. One is realizing a high blocking voltage and a low on-state voltage which are specifically important in high power application. The other is achieving faster switching characteristics and higher gate turn-off gain for high frequency and medium power application. The former is met by introducing a phosphorus redeposition annealing process¹⁾ to increase carrier lifetime in p-base, in addition to decreasing the p-base impurity concentration near the cathode-gate junction²⁾ to increase an emitter injection efficiency. The latter requirement is met by properly controlling current gains of two component transistors, including an anode-short structure.³⁾ In both cases, the major difficulty is to increase I_{ATO} , which denotes the maximum anode current to be interrupted without failure upon application of gate turn-off current. Undoubtedly, the most determining factor for I_{ATO} is the current crowding effect during the gate turn-off process.

In this paper, discussion will be made on single cathode element devices including a theoretical model and basic experimental results. In addition, a number of experimental results and overall device characteristics will be demonstrated on actual size whole devices.

In order to analyze the gate turn-off mechanism, a GTO charge-control model has been developed⁴⁾, including lateral currents through the conductivity-modulated base layers. According to the model, the whole device cross-section is laterally subdivided into a number of small segments, with interconnections of lateral base resistances. Each segment is described by a set of charge-control equations. This model provides computation results to figure out influence of several important design parameters, such as cathode pattern dimension, doping profiles and carrier lifetimes in two base regions. For example, a narrow p-base is shown to provide non-desirable condition for high current turn-off, because the current crowding occurs significantly, as a result of high interconnection resistances. In other words, the p-base layer conductance should be high enough for the excess carrier extraction to occur efficiently. Thus also follows that in case of rectangular pattern, the finger width should be small to realize a high p-base layer conductance. This is confirmed by an experiment on I_{ATO} vs. pattern width for single element devices.¹⁾

However entire pattern length criteria can neither be provided by the CAD-model, nor

electrical measurements on single element devices, because actually the current crowding in pattern length direction also occurs mainly due to fluctuation in impurity doping and lifetime. The problem was analyzed by introducing an infrared microscopic technology⁵⁾, with which carrier distributions are observed by detecting the infrared emission due to carrier recombination. During the storage time, conduction region length remains unchanged, but narrows itself in width. However, as the anode current begins to decrease, the conduction region is abruptly squeezed in the length direction. The final conducting spot is estimated around 100 microns in diameter. This value approximately corresponds to the diffusion length in p-base. These results lead to a conclusion that an extremely long emitter finger is undesirable.

From a circuit condition point of view, the gate voltage also has influence on the current crowding¹⁾. An experiment was made on switching two elements simultaneously with variation in gate voltage. It was found that decreasing the gate voltage intensifies nonuniformity in current distribution between two elements. In an extreme case entire current flows in one element. The gate turn-off capability can thus be improved by increasing the gate voltage, probably due to the drift effect in p-base through a high electric field near the cathode-gate junction during the fall time phase.

From measurements on actual multi-emitter devices, approximately linear relationship was found between I_{ATO} and the ratio $V_{J1}/\rho_{SPB}^{2)}$, where V_{J1} is the cathode-gate junction breakdown voltage and ρ_{SPB} , the sheet resistance in p-base. This fact implies that a large V_{J1}/ρ_{SPB} value contributes to the excess carrier removal of p-base. As a result, the current crowding is reduced, so that finally the gate turn-off capability is improved. This result is consistent with all previous results on single element. As a final conclusion, actual devices with 3 cm^2 cathode area were obtained having I_{ATO} of more than 600 A and gate turn-off gain of 5¹⁾.

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