A－3－7 150V High Voltage Linear IC Technology

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Introduction

In recent years, most of the circuits in consumer electronics equipment have been integrated on silicon chips with significant progress in integrated circuit technology. However, both high frequency front-end and high voltage output-end circuits are still made in discreate circuit styles, since conventional IC technology has not been able to integrate these circuits on silicon chips with resonable cost, performance, and reliability.

In this paper we report a novel IC structure, " Semi-Well Isolation Structure" (SWI), in which the epitaxial layer has two thicknesses on the same chip and a high voltage integrated circuit of up to 150V.

New IC Structure

The practical maximum operating voltage of consumer IC's has been limited to 60V or less. This restriction comes from the limit of increase in epitaxial layer thickness for high voltage devices. To increase the thickness of the epitaxial layer using conventional techniques requires a longer processing time and involves the following difficulties.

1) Fault density of epitaxial layer is inevitably increased due to longer time and high temperature of the isolation diffusion process.
2) Larger chip size due to increase in occupying area for isolation pushes up IC cost.

The new IC structure that solves these problems is shown in Figure 1. This structure has an epitaxial layer of two different thicknesses, while a conventional structure has only one thickness. The isolation regions are diffused in the thin portion of the epitaxial layer, so the processing time is the same as that for a conventional device. Devices are formed in the thick portion of the epitaxial layer, and the thickness of this layer can be designed to optimize breakdown voltage of the devices.

Two different thicknesses of epitaxial layers in same chip give us more freedoms in designing a high voltage IC.

Fabrication Process

The main points of the fabrication process of the SWI structure are shown in Fig. 2. The second step is to make the wells and the fifth step is to level the surface of the epitaxial layer. Both steps require an eching process to eliminate the need for selective epitaxial growth or silicon surface polishing processes which may limit the yield. After the sixth step, conventional high voltage linear IC processes are used.

High Voltage Technology

Maximum voltage of the conventional high voltage IC is also limited by increase of silicon

surface electric field strength which is caused by metalization lines on the chip. The two types of the degradations of p-n junction breakdown voltage due to metalization lines are considered in Fig. 3. The breakdown voltage of both p-type diffusion regions is about 110V in conventional high voltage linear IC structure. Thicker silicon oxide film and ion-implanted layer are introduced to prevent the degradation of breakdown voltages.

A 150V high voltage IC is easy to design with this technology.

Color TV Vertical Out-put IC

We have developed a color TV vertical deflection out-put IC operated by a transformerless voltage source (115v). It is the first integrated circuit operating in this voltage range commercially available so far. A microphotograph of the chip is shown in Fig. 4. This IC consists of several npn, pnp transistors and resistors which can withstand 200V.

Conclusion

A 150V linear IC was developed by using the Semi-Well Isolation Structure and high voltage technology related to metalization lines on the silicon chip.

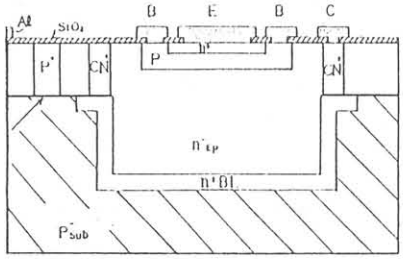
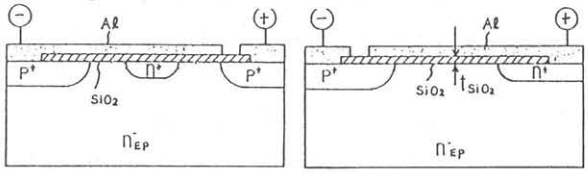


Fig. 1 Cross-sectional view of SWI structure



(a) channel stopper case (b) reverse field-plate case

Fig.3 Cross-sectional view of two kinds of metalization

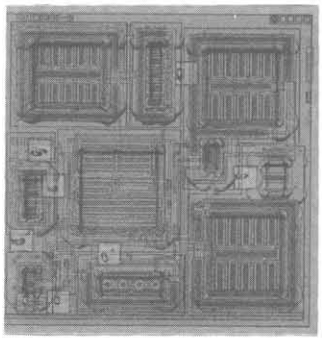
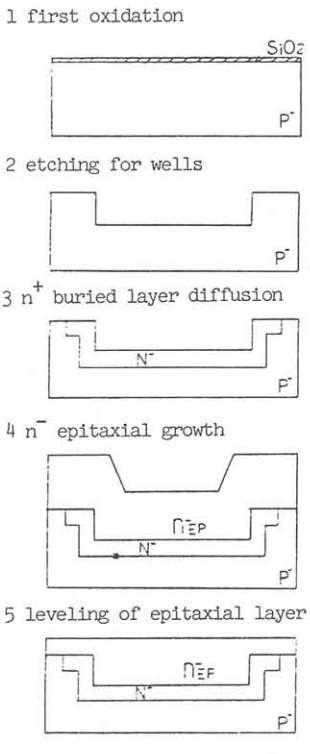


Fig.4 Photomicrograph of the chip



6- conventional high voltage linear IC process

Fig. 2 Fabrication steps for SWI structure