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High Speed $MoSi_2$ gate CMOS/SOS Devices

Yoshihisa MIZUTANI, Kenji MAEGUCHI, Tohru MOCHIZUKI
Minoru KIMURA, Mitsuo ISOBE, Yukimasa UCHIDA and Hiroyuki TANGO

Semiconductor Device Engineering Laboratory
TOSHIBA CORPORATION

Komukai-Toshiba-cho, Kawasaki, JAPAN

Short channel CMOS/SOS device fabrication using poly-silicon gate technology has been attempted[1][2]. However, from the view point of practical realization of very high speed, high packing VLSI/SOS, several problems have not been solved yet. Those are how to suppress the anomalous drain currents, i.e. punch through current of N and PMOS/SOS FET and back side channel current of NMOS/SOS FET, how to precisely control the threshold voltages, and what other materials, instead of polycrystalline silicon, we can adopt for the gates and interconnections for better circuit performance. In order to suppress the anomalous drain currents and to precisely control the threshold voltages, double ion implantation under the gate should be most practical technology for downward scaled CMOS/SOS devices[3]. Use of polycrystalline silicon for the gates and interconnections should be encountered with some limitations because of its higher sheet resistivity and its larger grain size which should be formidable for fine pattern difinition. Refractory metals such as Mo have been proposed[4], but they are generally poor compared with poly-silicon regarding the resistance to withstand chemical reagents and oxidizing ambients used in LSI processing. Silicides of refractory metals such as $MoSi_2$ have been proposed and various investigations pursued show that its meets all of the requirements which were mentioned above[5]. This paper describes the design and characterization for very high speed, CMOS/SOS devices utilizing $MoSi_2$ gate technology with effective channel length of 1.5 μm. Moreover, a new high speed, lower power 4K (4K x 1) - bit CMOS/SOS RAM are described.

$MoSi_2$ films ere deposited on oxidized silicon films on sapphire by planar magnetron type sputter apparatus in Ar (3.5×10^{-3} torr) at room temperature[5]. The sputtering target was made of hot pressed $MoSi_2$ compounds. The deposition rate was about 10 A/sec at sputtering power of 700 W. As shown in Fig. 1, sheet resistivity of 3.5 $\Omega/\square$ was obtained after 1000°C annealing in N_2 for 30 min. for the thickness of 2200 A. Photolithography was performed to define the 2 μm gates and interconnections. Chemical Dry Etching (CDE) method[6] is successfully used to etch $MoSi_2$ as shown in Fig. 2, which the etching rate of $MoSi_2$ is approximately 1/3 of the poly-silicon etching. The as-deposited $MoSi_2$ is amorphous and prolonged after high temperature annealing results in polycrystalline structure with grain size of ~ 2000 A, which is still smaller than that of polycrystalline silicon, and thus makes it easy to define fine patterns.

CMOS/SOS devices were fabricated on 0.7 μm thick SOS wafer by $MoSi_2$ gate technology. Gate oxide thickness was 500 A. Double ion implantation of deep boron and shallow phosphorus for n-channel and deep phosphorus and shallow boron for p-channel were applied to the channel region. Using $MoSi_2$ gate, both n- and p-channel enhancement mode FET can be easily made because of the higher work function of $MoSi_2$ by 0.5 eV compared with that of n^+-poly-silicon gate. Use of enhancement mode FET's for both channels is beneficial to adjust threshold voltage and to reduce leakage current because the epitaxial layer near the substrate with higher defect density can be remained as neutral region.
Measured threshold voltage shifts due to so-called short channel effect are shown in Fig. 3, and punch through or breakdown voltages are shown in Fig. 4. These results clearly show that, as the minimum dimension for both NMOS and PMOS FET, L_{eff} = 1.5 μm appears to be practical as far as the power supply is 5 volts.

Fig. 5 shows the downward scaled $MoSi_2$ gate CMOS/SOS delay time measured using 19-stage ring oscillator. Stage delays of 167 psec and 255 psec with power dissipation of 6.5 mW and 3.6 mW for L_{eff} = 1.0 μm and 1.6 μm devices were obtained at V_{DD} = 5 V. A 4K (4K x 1) - bit CMOS/SOS RAM with the standard six-transistor CMOS static RAM cell has been successfully fabricated. The cell size and the chip size are 36 x 36 μm^2 and 3.23 x 4.19 mm^2, respectively (Fig. 6 and Fig. 7). Typical access time was 20 nsec with the power dissipation of 250 mW at V_{DD} = 5 V, which was accomplished by the reduction of word line propagation delay by the amount of 6 nsec by using $MoSi_2$ instead of poly-silicon.

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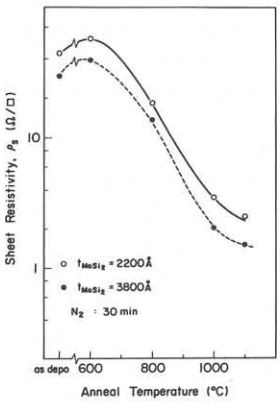

Fig. 1. $MoSi_2$ sheet resistivity annealing effect.

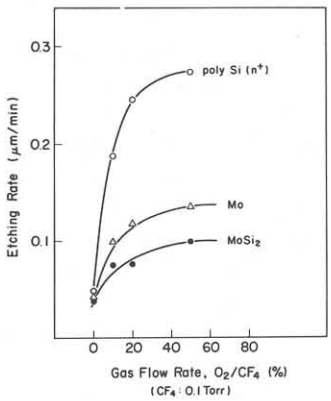

Fig. 2. Etching rate of $MoSi_2$, Mo and n^+ poly-silicon by CDE method.

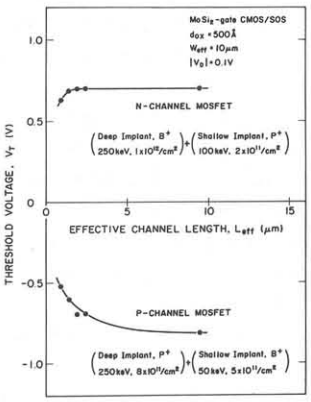

Fig. 3. N-and PMOS/SOS FET threshold voltage vs effective channel length.

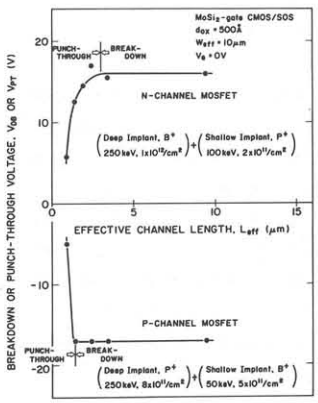

Fig. 4. Breakdown or punch-through voltage vs N-and PMOS/SOS FET effective channel length.

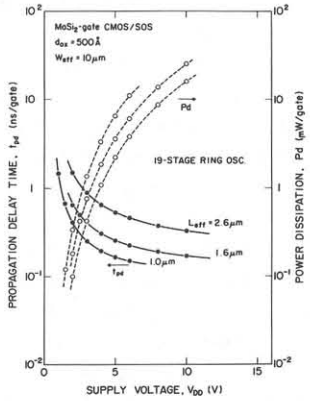

Fig. 5. $MoSi_2$ gate CMOS/SOS stage delay and stage power dissipation vs supply voltage.

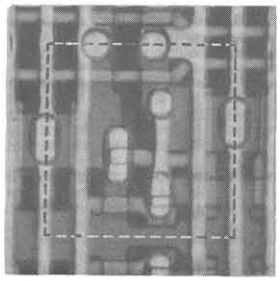

Fig. 6. Microphotograph of the CMOS/SOS RAM cell.

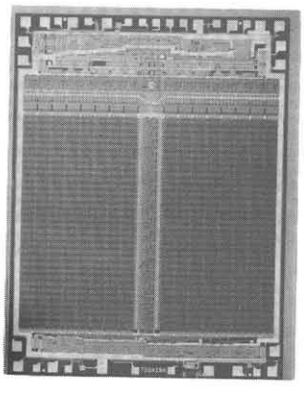

Fig. 7. Microphotograph of the 4K CMOS/SOS RAM chip.