A－4－2 High Speed 4 k bit Static RAM with Silicide Coated Wiring

M. Morimoto, M. Sugimoto, K. Terada, K. Takahashi, T. Ishijima, H. Muta and S. Suzuki

Central Research Labs.,

Nippon Electric Co., Ltd., Kawasaki

A high speed, fully static, 4096 word by one bit Random Access Memory has been developed, using short channel MOS FETs with PtSi coated polysilicon gates as active devices and PtSi coated n^+ diffusion layer as low resistive wiring. The present RAM was operated on a single 5 ±1 volt power supply. Its typical performances are 20 nsec address access time, 22 nsec chip select access time, 500 mW operating power and 50 mW stand-by power.

Figure 1 shows main fabrication process for an E/D inverter with a power reduction switch integrated in the RAM as a basic circuit. High resistive P type substrate (40 Ω cm) was chosen to reduce junction capacitances. Enhancement type short channel MOS FETs with L_{eff}=1.3 μm were used as drivers. Their threshold voltages were appropriately adjusted by double boron-ion implantation without emphasizing short channel effects. Threshold voltages for depletion type load MOS FET, 0 volt threshold power reduction switch and cell load MOS FET were individually adjusted by arsenic channel implant doses.

As is shown in Figs. 1 (a) and (b), PtSi film coated on gate polysilicon and n^+ wiring region is self-aligned by using Si_3N_4 mask without any additional photomasks. Therefore, the PtSi coating process is fundamentally compatible with the conventional silicon gate MOS technology. Sufficiently low sheet resistivity (2 ∿ 3 Ω/□) was achieved. As PtSi coating processes are carried out at less than 600 °C annealing temperature, the shallow arsenic implanted layer for source and drain electrodes is not influenced. MOS FET reliability with PtSi coated polysilicon gate was confirmed by a BT test (V_G=10 V, 150 °C) for a period of 1000 hours.

In addition to the above mentioned optimizations on fabrication process and devices for high speed operation, following improvements in circuit design were also determined; (1) Address inverter circuit with E/E push-pull output stage for low power operation, (2) Low power dualized main sense amplifiers, (3) Output buffer with boot-strap drive stage for fast pull up and (4) On chip substrate bias generator.

Figure 2 is a microphotograph of the present RAM. Chip size and cell size are 2.35 mm x 4.3 mm and 23 μm x 42 μm, respectively. Figure 3 shows the address input and data output waveforms. Measured address access time was 20 nsec. It was also confirmed that the address access time dependency on physical address along a word line was negligible.

Typical characteristics for 4 k RAM are summarized on Table 1.

The authors are grateful to Drs. S. Asanabe, D. Shinoda and N. Kawamura for their continuous encouragement during this work, and to Messrs. I. Nagashima, T. Takegawa, Y. Kurogi, and K. Kamimura for their assistance in the fabrication process.

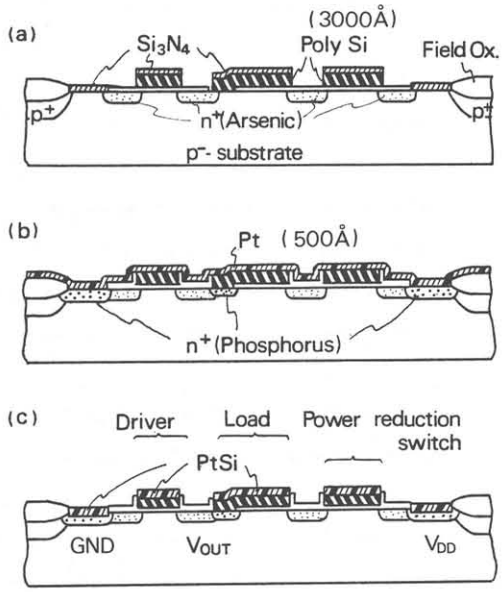

Figure 1 Main fabrication process for an E/D inverter

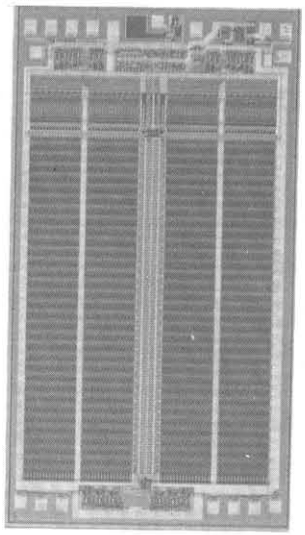

Figure 2 4 k bit static RAM chip microphotograph

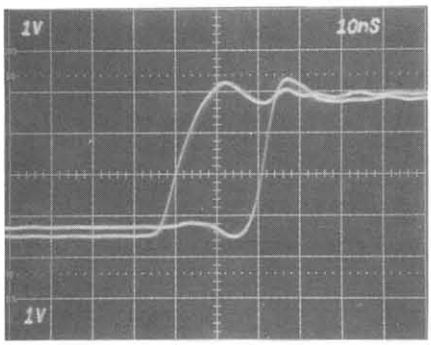

Figure 3 Address input signal and data output signal waveforms (V_{DD}=5 V)

Technology:	N-channel Si gate MOS, double boron -ion implanted short channel MOS FET, PtSi coated low resistive poly silicon and n^+ layer wiring
Pins:	18 pins
Chip size:	2.35 mm x 4.3 mm
Cell size:	23 μm x 42 μm
Organization:	4096 word by one bit, fully static
Cell structure:	6 Tr. static cell
Power Supply:	5 volt single, on chip substrate bias generator (V_{SUB}= -2V)
Signal level:	TTL compatible
Address access time:	20 nsec
Chip select access time:	22 nsec
Power dissipation:	500 mW operation 50 mW stand-by

Table 1 4 k RAM typical characteristics summary