A－4－3 Custom LSI Process with a Micron Geometry, Partially Using Electron Beam Direct Writing

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A demand for custom LSIs, which tends to a large variety in small production numbers, has become stronger as VLSI technology becomes better established. For example, there are ROM (read only memory) and PLA (programmable logic array) in demands, which are produced by making pattern alteration of only one mask level. Recently, electron beam exposure technology has been developed for advanced lithography. An available potentionality of electron beam direct writing seems to be concentrated rather on pattern generation flexibility although its high resolution was emphasised hitherto[1]. On the other hand, a reduction-projection exposure system, whose images are photoreduced, stepped and directly exposed on the wafer, can be used for less than 2 μm resist images and high overlay accuracy, which are required for VLSI level. Custom LSI process partially using electron beam direct writing has been applied to fabrication of a higher packing density 512 kbit ROM with a micron geometry.

The 512 kbit ROM was fabricated using n-channel poly-Si gate MOS process. In this lithography, the 10 to 1 direct stepper (4800 DSW) was used[2], except for a data writing step. Electron beam exposure system (JBX-6D) was employed in data writing due to the through-hole patterning. Using two different exposure systems, it is important that the alignment procedure for the direct stepper should match electron beam exposure system requirements. Alignment for electron beam exposure, which is made using cross matching symbol, handles wafer rotation and field correction. The matching symbol size and location are decided at the mask layout design and stepper exposure program. The matching symbols were delineated by the stepper and replicated by etching the substrate Si into 1.5 μm depth. Figure 1 shows the patterned symbol position within a 4 inch wafer. The average overlay error of electron beam exposure to underlying pattern was less than 0.3 μm between wafers. AZ-2400, a positive electron beam resist with 3×10^{-5} C/cm^2 typical sensitivity, was used for contact hole patterning. AZ-2400 was not so sensitive for electron beam, but had a sharp pattern profile and comparatively large tolerance for dry etching. Resist pattern size accuracy was ±0.15 μm. Exposure time, including matching symbol detection and stage movement, was 60 seconds per chip. AZ-1370 and AZ-1350J were used as photoresist. The exposure time for the stepper was about 80 seconds per wafer, including 81 chips. This direct stepper had an overlay accuracy of less than 0.3 μm. Table 1 shows a typical example of the overlay results. The dry processes using anisotropic etching were applied for LSI manufacturing. Namely, SiO_2, Si_3N_4 and poly-Si were etched using a planar reactive sputter techniuqe with CF_4-H_2 and CCl_3F gases[3]. Al was also etched by utilization of a planar plasma etcher with a CCl_4 gas.

A 512 kbit ROM chip is organized as eight 64 kbit ROM blocks. The decoders for this ROM are operated by static NOR circuit, and 8 bit outputs are read out in parallel. The minimum ground rules

are as follow: device area spacing is 1.2 μm, poly-Si gate length is 1.8 μm, contact hole is 1.4 μm x 1.4 m and metal linewidth is 3.2 μm. Data writing, using electron beam lithography is achieved by contact hole opening of the drain region in the cells. The contact holes are formed just before a final metallization to shorten the production turn around time. They are dèsigned to lie on the phosphorus-doped poly-Si pedestals, decreasing the isolation insulator step. Memory cell size and chip size for the ROM are 5.2 μm x 8.4 μm and 6.6 mm x 8.9 mm, respectively.

The device operation was confirmed by displaying chinese ideographs on the CRT. A part of the Chinese ideographs is shown in Fig. 2. Typical address time and power dissipation for the fabricated ROM was 400 nsec and 800 mW, respectively, at 5 V single voltage with TTL compatibility. A microphotograph of the 512 kbit ROM chip is shown in Fig. 3.

Direct stepper lithography partially using electron beam direct writing was confirmed to be effective for the custom manufacturing LSIs with a micron geometry. Such a method seems applicable to another mask level instead of the contact hole.

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1) E. Arai, T. Ogawa, N. Ieda, K. Kiuchi, K. Iwadate and K. Takeya, Japan. J. Appl. Phys., Suppl. 18-1 (1979) 295
2) G.L. Resor, Microelectronics Journal, 10, (1979) 18
3) N. Endo and Y. Kurogi, IEEE 2nd VLSI Special Issue, to be published

Table 1 Example of the overlay results within a wafer

	CH vs GS		CH vs GR		GS vs GR	
	X	Y	X	Y	X	Y
Above	-.1	.05	-.05	0	0	0
Center	-.2	.05	0	.1	.15	0
Below	-.35	.05	-.05	.1	.35	.05
Left	-.15	-.25	0	.05	.2	.25
Right	-.15	.1	.2	.25	.3	.1
Aver.	-.19	0	.02	.1	.2	.08
σ	.086	.126	.093	.084	.122	.093

(micron units)

GR guard ring
GS gate poly-Si
CH contact hole

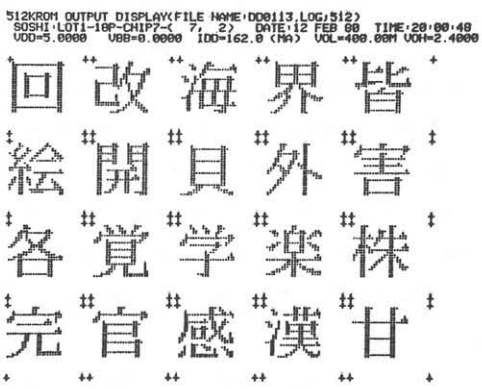

Fig. 2 A part of the Chinese ideographs

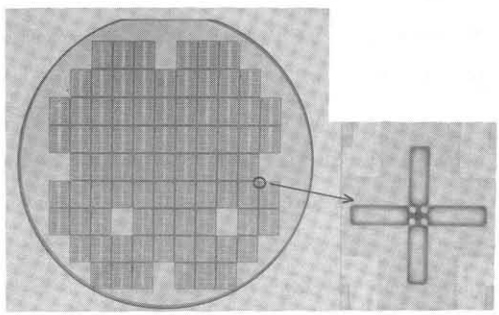

Fig. 1 Microphotograph showing the patterned symbol position in 4 inch wafer

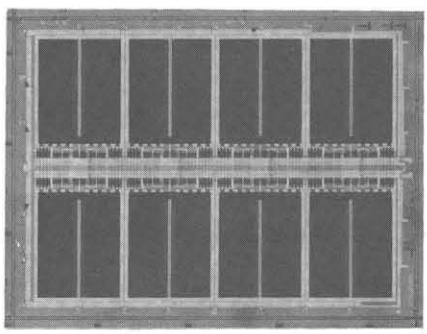

Fig. 3 Microphotograph of 512 kbit ROM chip