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Soft Error Improvement in MOS RAM's by the use of Epitaxial Substrate.

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The soft error caused by alpha particles is one of the serious problems in scaled dynamic MOS RAM's.[1] This work presents a method to improve the soft error by the use of p epitaxial layer on p_{++} silicon substrate.

Fig.1 shows the soft error rate vs. memory cycle time of the 64K-bit dynamic MOS RAM. Soft error rate in the epitaxial substrate is 10 to 100 times as small as the substrates with uiform resistivity of 3Ω-cm, 10Ω-cm and 20Ω-cm.

Fig.2 shows the cross sectional view of the MOS RAM. The data of soft error rate were obtained by using Americium 241 alpha sources on the MOS RAM.

The impurity profile of epitaxial substrate is measured by spreading resistance technique as shown in Fig.3.

Depletion layer width W_d from n_{++} diffused layer in several substrates is shown in Fig.4. The W_d in epitaxial substrate at a voltage of 8 V is nearly equal to that of the substrate of 3Ω·cm resisitivity. To clarify the relation between soft error rate and collected charge in diffused bit line of 64K-bit RAM, we calculated the Q_α of 4 different kinds of substrate. Q_α is obtained by (1).

$$Q_\alpha = Q_{\alpha A} + Q_{\alpha B} \quad \text{----------(1)}$$

where Q_α is total charge deposited by diffusion away from a particle track, $Q_{\alpha A}$ is total charge in depletion layer and $Q_{\alpha B}$ is total charge beneath the depletion layer.

Assuming the charge density ρ_o to be uniform, we obtain

$$Q_{\alpha A} = \rho_o wd \quad \text{----------(2)}$$

Collecting current density j(r,t) is given by the following equation[2]

$$j(r,t) = j_o \lambda^{-3} \exp(-r^2/R^2\lambda^2)[1-\exp(-\lambda^2)] \quad \text{---------(3)}$$

where $\lambda^2 = t/t_o = 4Dt/R^2$ t:time [sec] R:track length [μm]

r:distance from the particle entarance point [μm]

We can obtain $Q_{\alpha B}$ by integrating (3). Soft error can occur during a time t of 50 ns in sense amplifier. Fig.5 shows the normalized charge K within radius r of the particle entrance point from 20μm vertical track for 50ns. In this case, we obtain

$$Q_{\alpha B} = \rho_o RK = 20K\rho_o \quad \text{----------(4)} \quad \text{and} \quad Q_\alpha = (wd+20K)\rho_o \quad \text{----------(5)}.$$

The calculated Q_α and collecting efficiency S are summarized in table 1, and soft error rate decreases with the increase of S^{-1} as shown in Fig.6.

In conclusion, the improvement of soft error in 64K-bit dynamic MOS RAM was made by using the epitaxial substrate, which is explaind by the smaller collecting efficiency.

References

[1] T.C.May and M.H.Woods:IEEE Trans. Electron Devices, Vol. ED-26 (1979) 2.

[2] Scott Kirkpatrick,IEEE Trans. Electron Devices, Vol. ED-26 (1979) 1742.

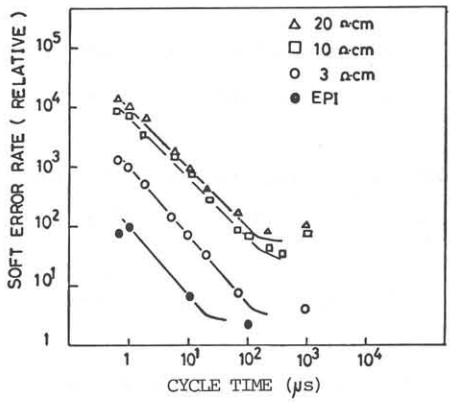

Fig.1 Soft error rate vs. cycle time

(r=10 m, r/R =0.5)

SUBSTRATE	Q_α	S	S^{-1}
20 Ω·cm	11.1 ρ_0	1	1
10 Ω·cm	10.1 ρ_0	0.91	1.09
3 Ω·cm	8.9 ρ_0	0.80	1.25
EPI	7.7 ρ_0	0.69	1.44

Table 1 Calculated Q_α & S

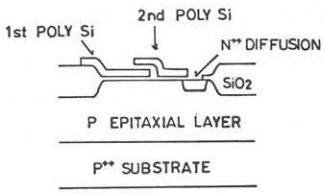

Fig.2 Dynamic MOS RAM structure used in this experiment

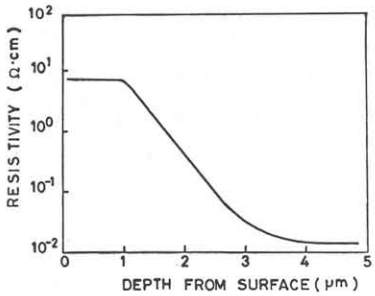

Fig.3 Impurity profile of epitaxial substrate

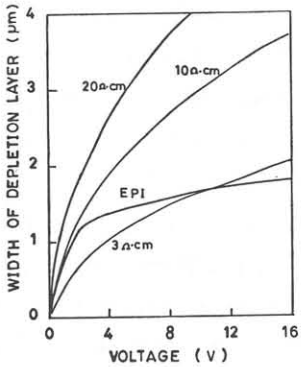

Fig.4 Depletion layer width vs. applied voltage

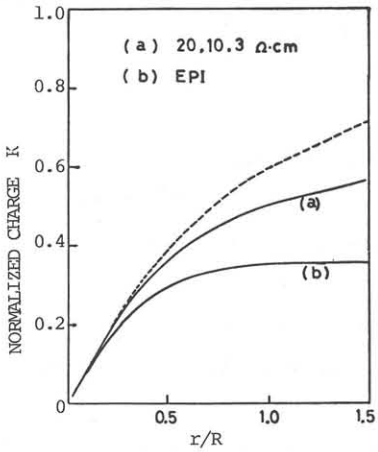

Fig.5 Collected charge vs. r/R

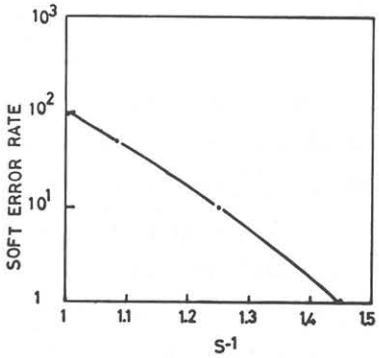

Fig.6 Soft error rate vs. S^{-1}