A－4－6 Flat Emitter Transistor with Self-Aligned Base

T. Fujita, H. Yamada, T. Takemoto, T. Komeda
Semiconductor Research Laboratory, Matsushita Electric Industrial Co., Ltd.
3-15 Yagumo-Nakamachi, Moriguchi-Shi, Osaka 570, Japan

A flat emitter transistor with a self-aligned base has been developed to realize a high speed and low power dissipation bipolar LSI.

This transistor has a flat bottom emitter and eliminates parasitic capacitance in the side wall. In conventional fine pattern emitters, the bottom face tends to take an oval shape.[1] Accordingly, a uniform narrow active base cannot be formed right below the emitter. Moreover, the parasitic capacitance exists in the side wall. By contrast, the flat emitter makes possible such a uniform narrow active base together with lowered C_{TE} due to nonexistence of the side wall capacitance. Consequently, high cut-off frequency (f_T) can be obtained at low current. The transistor also has an inactive base of high impurity density (self-aligned base) formed extremely near the emitter region. As a result, the base resistance can be lowered even though single line contact is used. This base contact structure enables the reduction of C_{TC} and C_{TS}. Further, a resistor with high sheet resistivity can be simultaneously formed without increasing the number of process steps.

The process outline is as follows. (See Fig. 1)
First, an n^+ buried layer and a boron-doped buried layer for the upward isolation are formed in a p-type silicon substrate before a 1Ω-cm n-epitaxial layer is grown. Second, the entire isolation and a collector sink are formed. Then, a nondoped 0.2μm thick polysilicon is deposited after opening windows for the base and registor regions. Subsequently, arsenic is diffused into the both regions through the polysilicon. Thus a 0.2μm n^+ region is formed as shown in Fig.1-(a). Using an emitter pattern mask of 600Å Si_3N_4 film, the regions of silicon doped arsenic are removed by wet etching. Consequently, an n^+ emitter region with a flat bottom is formed as shown in Fig.1-(b). Then a silicon layer is oxidized by using the Si_3N_4 mask. Boron is ion-implanted with an acceleration energy of 160 kev and a dose of 1×10^{13} ions/cm^2 through the SiO_2 film. This process forms an uniform active base and a buried high sheet resistance simultaneously. [Fig.1-(c)] The width of the base is 0.2μm and the resistivity of the buried resistance is 2.8 kΩ/□. Further, boron is again ion-implanted with an acceleration energy of 60 kev and a dose of 1×10^{15} ions/cm^2. But this time, the buried resistance except the contact region of the registor is covered with a photoresist. As a result, the inactive base region (self-aligned base) with a sheet resistivity of 135 Ω/□ and

the contact region of resistor are formed simultaneously. [Fig.1-(d)] After all contact windows are opened, electrode bumps are fabricated.

Table 1 represents the characteristics of the flat emitter transistors with emitter sizes of $2\times4\mu m^2$ and $2\times16\mu m^2$. Fig.2 shows the f_T-I_C characteristic of the $2\times16\mu m^2$ transistor. Fig.3 is a photograph of a 1/256 divider chip with low power dissipation. The divider operates at frequencies up to 1.1GHz and its output waveform is shown in Fig.4. The power dissipation of the divider is 110mW, being one fifth that of the conventional divider.

As described so far, the flat emitter transistor with a self-aligned base is applicable for high speed and low power dissipation bipolar LSI.

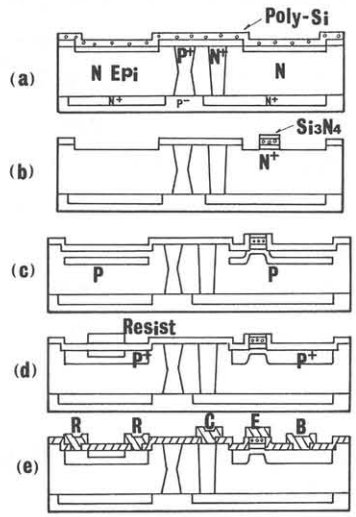

Fig.1. Fabrication process of flat emitter transistor with self-aligned base

Emitter size	$2\times4\ \mu m^2$	$2\times16\ \mu m^2$
f_T max	3.7 GHz	5 GHz
C_{TE}	0.008 pF	0.032 pF
C_{TC}	0.043 pF	0.1 pF
C_{TS}	0.1 pF	0.14 pF
$r_{bb'}$	240 Ω	115 Ω
H_{FE}	150	150
BV_{CEO}	18V	18V
BVEBO	4.5V	4.5V
BV_{CBO}	35V	35V

Table 1. Characteristics of $2\times4\mu m^2$ and $2\times16\mu m^2$ flat emitter transistors

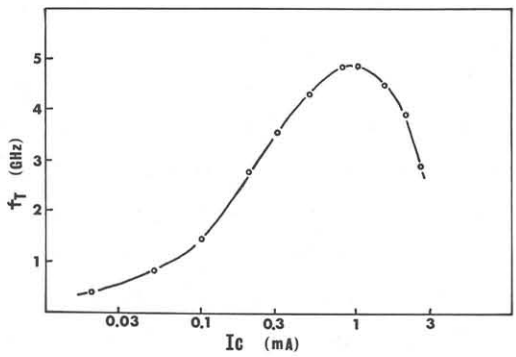

Fig.2. Cut-off frequency versus collector current of flat emitter transistor with $2\times16\mu m^2$ emitter size.

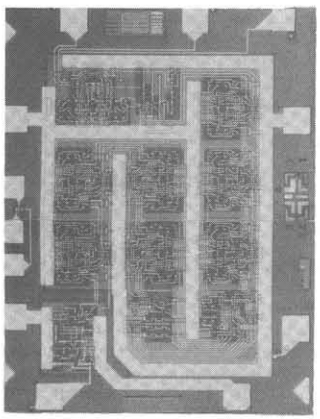

Fig.3. Photograph of 1/256 divider chip

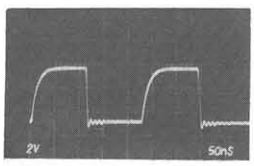

Fig.4. Output waveform of 1/256 divider

(1) T. Irie: I.E.C.E. of Japan (1967) p39