A－4－7 High Speed Bipolar ICs Using Super Self-aligned Process Technology

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To realize high speed and high packing density bipolar ICs with small power dissipation, many methods have been studied[1),2),3)]. Here, we report a new bipolar integrated circuit structure making full advantages of self-aligned process. This technology is called Super Self-aligned process Technology or SST. A cross sectional view of the integrated transistor obtained by using SST is shown in Fig. 1-(f). The distinctive features of this structure are as follows.

(1) The base contact region consists of P^+ polysilicon with submicron width, which is formed uniformly around the emitter area.

(2) Only one mask is enough to form base-collector junction, emitter-base junction and base P^+ polysilicon electrode.

The fabrication steps are as follows.

(a) The process steps are the same as for the conventional bipolar ICs until an isolation layer is formed. Subsequently, multilayers shown in Fig. 1-(a) are formed. Unnecessary polysilicon layer is selectively oxidized.

(b) The emitter and collector windows are opened and the CVD SiO_2 film is side etched.

(c) The Si_3N_4 film shadowed by the overhanging edge of the boron doped polysilicon layer is removed selectively, and again the boron doped polysilicon layer is deposited.

(d) Polysilicon deposited in process (c) is removed by ion milling.

(e) Boron is implanted in the base area. The thermal oxidized film with 0.3 to 0.5μm thick is formed.

(f) The Si_3N_4 film and SiO_2 film for emitter area is removed. Then, the transistor is completed by using standard processes.

The above structure has following advantages. As the active regions of transistor can be formed by using only one mask, base regions can be reduced about 1/4 to 1/6 compared with that of conventional transistor. Therefore, the parasitic capacitance can be reduced. The cross sectional view of this structure after etching the boron doped polysilicon layer by ion milling is shown in Fig. 2. Several device parameters of the experimental integrated transistor are shown in Table 1. To evaluate the performance of SST, a 51-stage ring oscillator with NTL has been fabricated as shown in Fig. 3. The oscillation waveform is

shown in Fig. 4. The propagation delay time was 70 to 85 ps/gate and power delay product was 42 to 51 fJ/gate. It has been confirmed SST is the effective to realize bipolar ICs with low power, high speed as well as high packing density.

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1) T. Sakai et al., ISSCC Dig. Tech. Paper, pp. 196-197, 1979.

2) K. Okada et al., IEEE J. Solid-State Circuits, vol. SC-13, pp. 693-698, 1978.

3) I. Ishida et al., IEDM, pp336-339, 1979.

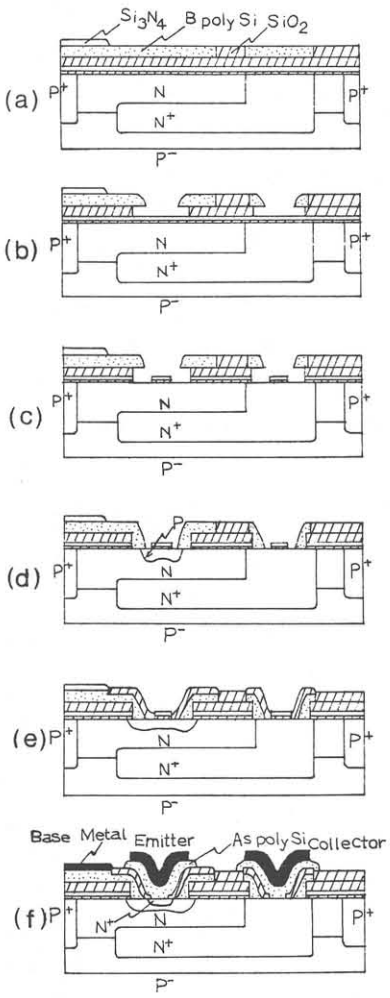


Fig. 1 Fabrication process.

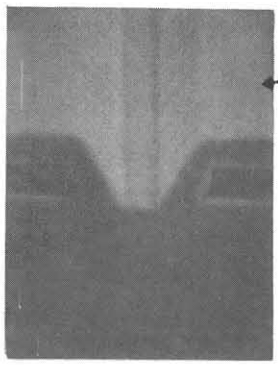


Fig. 2 SEM micrograph of the base polysilicon electrode.

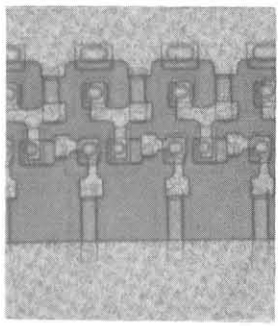


Fig. 3 Photograph of NTL gates 51-stage ring oscillator.

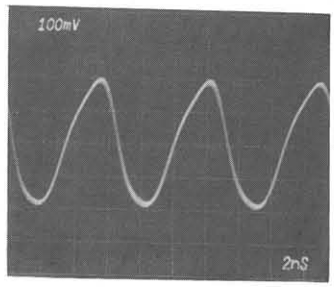
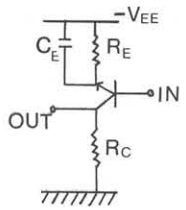


Fig. 4 Oscillation waveform of a 51-stage ring oscillator.



Emitter base junction capacitance	32 fF
Base collector junction capacitance	11.4 fF
Isolation capacitance	51 fF
Emitter area	2x3 μm^2
Base area	4x5 μm^2

Table 1 Device parameter.