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# A High Performance $I^2L$ Compatible with Sub-nanosecond ECL devices

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This paper describes a new approach for realizing a high performance $I^2L$ and a sub-nanosecond ECL circuit simultaneously on a single chip. Significant features of such a technology are a buried base structure for $I^2L$ gate and an implanted self-aligned contact (ISAC) structure[1] for ECL circuit combined with dielectric isolation technology. Following typical data are achieved with these advanced structures on a chip for a 4 $\mu$m design rule ; (1) a toggle frequency of $I^2L$ flip flop circuit is 73 MHz with $10^{-4}$ Watt/Gate power, (2) a power-delay product of $I^2L$ gate is 45 fJ for the fan-out of 3, (3) an ECL gate delay time of 0.68 nsec is obtained with a swithcing current of 0.46 mA from 11 stage ring oscillators on the same chip.

## ISAC ECL and Buried Base $I^2L$ compared with Graft Base $I^2L$

A sub-nanosecond ECL device was achieved with dielectric isolation, 1.8 $\mu$m thick n-type epitaxy, shallow junctions of fully ion implantation and ISAC emitter. Fig.1 shows cross-sections of an ISAC ECL npn transistor, a graft base $I^2L$ inverter and a buried base $I^2L$ inverter. The intrinsic base of buried base $I^2L$ was formed by boron ion implantation after the formation of buried emitter and by up-diffused boron into epi layer, which covered the buried emitter. The collector area Sc of buried base I2L was larger than that of graft base I2L with ISAC structure as the same collector contact area. The large value of the effective upward current gain $\beta_{eff}$ was obtained in the buried base $I^2L$ by the large $Sc/S_B$ and by the optimization of intrinsic base profile as shown in Fig.3. Then, the minimum delay time $t_{pdmin}$ decreased slightly with decreasing the collector contact area, as shown in Fig.2. On the other hand, the $t_{pdmin}$ of the graft base $I^2L$ increasing the collector contact area also shown in Fig. 2. Because, the value of $\beta_{eff}$ in the graft base $I^2L$ was smaller than that of the buried base $I^2L$ and decreased abruptly with decreasing the collector contact area. Therefor, the packing density of the graft base $I^2L$ with ISAC structure would be limited by the operation speed of a device. In case of the buried base $I^2L$ with ISAC structure, a small gate area of 650 $\mu m^2$ was carried out with a power-delay product of 45 fJ and a $t_{pdmin}$ of 5.2 nsec, as shown in Table 1.

## Buried Emitter Impurity dependence on Device Speed

Fig.3 shows vertical depth profiles of buried base structure. In case of the arsenic buried emitter, the emitter junction was formed at the high impurity concentration as compared with the antimony buried emitter. The buried base $I^2L$ gate with the arsenic buried emitter resulted in higher speed than that with the antimony buried emitter, as shown in Fig.4, because of the reduction of the hole storage in the emitter region. However, a power-delay product at low power level was found to be larger in the arsenic buried emitter about 1.3 times than that in the antimony buried emitter.

Walled Collector Type Buried Base $I^2L$

Fig.5 shows SEM photograph of a wallled collector type buried base $I^2L$ gate. The $t_{pdmin}$ decreased on the straight with decreasing the collector contact area, as shown in Fig.2. So, such $I^2L$ gate would be achieved with a large packing density and a high speed operation. Device characteristics of various structure $I^2L$ gates are summarized in Table 1. By a walled collector type buried base $I^2L$ gate, a gate area of 400 $\mu m^2$ and a $t_{pdmin}$ of 2.9 nsec were carried out for a 3 $\mu$m design rule, as shown in Table 1.

1) Y. Akasaka, et al., 1978 IEDM 8-4 p.189(Washington, 1978)

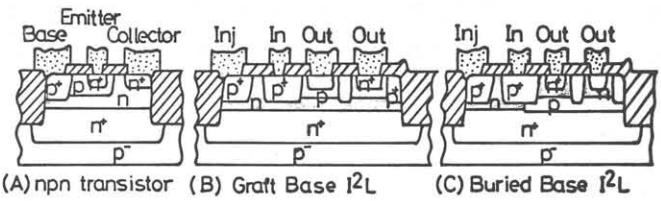


Fig. 1. Schematic cross-sections of npn transistor used for ECL circuit and $I^2L$ inverter

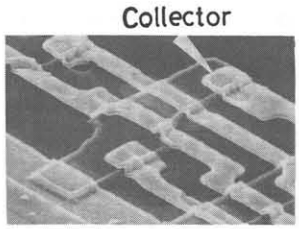


Fig. 5. SEM photograph of walled collector type buried base $I^2L$ gate.

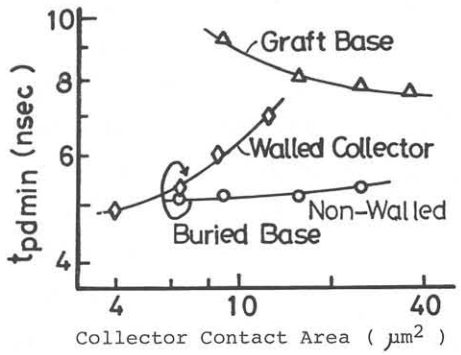


Fig.2. Collector contact area dependence on minimum delay time in various structures $I^2L$ gates (FO:3).

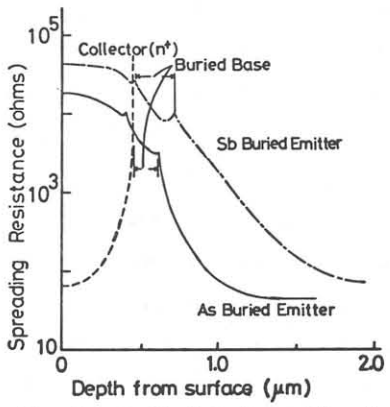


Fig. 3. Vertical depth profile of buried base structure.

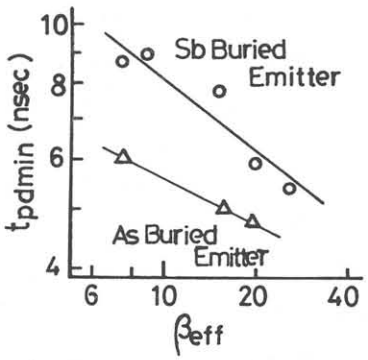


Fig. 4. $t_{pdmin}$ versus $\beta_{eff}$ for buried base $I^2L$ gate.

Table 1. Device performance in various $I^2L$ gates (FO:3) compatible with ECL circuit.

| Device structure | Graft base | Buried base | Walled type |
|---|---|---|---|
| Gate area | 780 $\mu m^2$ | 650 $\mu m^2$ | 400 $\mu m^{2*}$ |
| Buried emitter impurity | As | Sb | As |
| $t_{pdmin}$ | 8.5 nsec | 5.2 nsec | 2.9 nsec |
| Pd X $t_{pd}$ | 110 fJ | 45 fJ | 40 fJ |
| $f_{max.}$ ** | 21 MHz | 73 MHz | - |

*: 3 $\mu$m design rule. **: Maximum toggle frequency.