B－3－2 Planar GaAs ICs Using Multiple Localized Ion-Implantation

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The family of planar GaAs ICs has been developed by using a multiple localized ion-implantation technique. The minimum propagation delay of 90 ps from a 5-stage ring oscillator and the maximum counting frequency of 2.2 GHz from a binary frequency divider were obtained.

The basic logic circuit in the ICs consists of normally-on GaAs MESFETs and Schottky diodes as shown in Fig.1. The gate of the FET is 1.0 μm long and 20 μm wide. The area of the diode is 18 μm x 4 μm. The active layers of the FETs and the diodes were made by implanting Si^+ into Cr-doped semi-insulating substrate with energy 140 KeV at dose of $1.73 \times 10^{12} cm^{-2}$ and 160 KeV at $3.49 \times 10^{12} cm^{-2}$, respectively. 2 μm thick photo-resist was used for ion-beam masking of localized implantation. After the two implants, annealing was carried out at $850^{o}C$ forming gas flow for 15 min with 1000 A thick SiO_2 encapsulation film. Figure 2 shows the resulting electron concentration profiles for both implants. The metal system used in the ICs were AuGe for ohmic contact and Ti/Pt/Au combination for not only interconnects but Schottky contacts. The use of Ti/Pt/Au gates could reduce drastically contact resistance between the gate and interconnecting metal compared with that of Al gates.

I-V characteristics of the FET and the Schottky diode fabricated by the multiple implants with the above condition are shown in Fig.3(A) in order to compare them with the characteristics shown in Fig.3(B) of the devices formed by single implant. In spite of the fact that the diodes were of same size, dependence of level shift voltage on current could be considerably decreased by using the multiple ion-implantation technique compared with the single.

Figure 4 is a photograph of the planar GaAs ICs family including 5-stage ring oscillators and binary frequency dividers.

The ring oscillator consists of five inverters and a buffer. At the maximum oscillation frequency with the supply voltages of 4.5 V and -3.0 V, the minimum propagation delay was calculated to be 90 ps and the power- delay product was 1.8 pJ.

The maximum counting frequency of the divider which consists of four NAND/AND gates and a buffer was 2.2 GHz as shown in Fig.5 with the supply voltages of 4.5 V and -3.0 V.

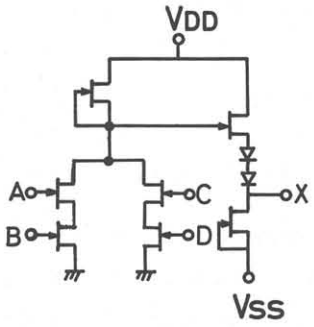

Fig.1. Basic logic circuit.

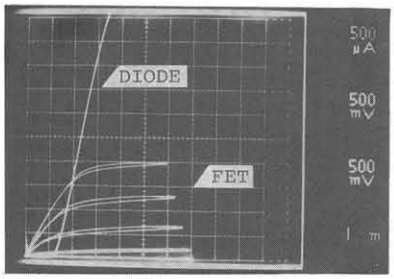

Fig.3(A). I-V characteristics of the FET and the diode by the multiple implants

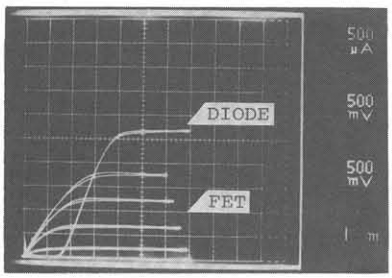

Fig.3(B). by the single implant.

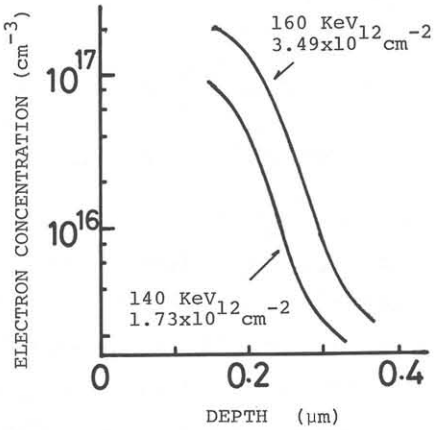

Fig.2. Resulting electron concentration profiles for both implants.

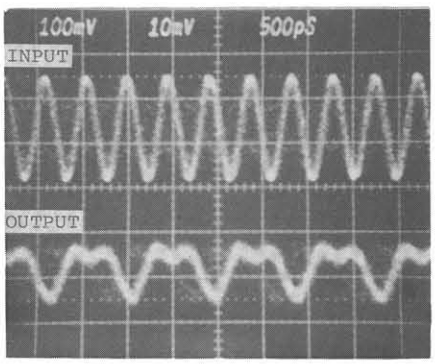

Fig.5. Response waveforms of the binary frequency divider for input frequency of 2.2 GHz.

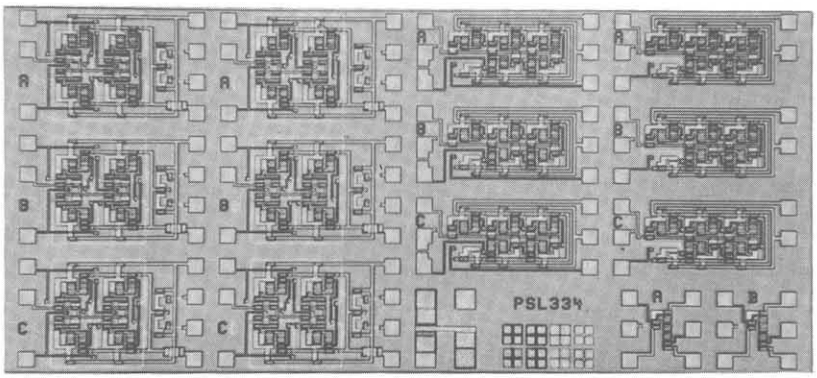

Fig.4. Microphotograph of the planar GaAs ICs family.

This work was partially supported by the Ministry of International Trade and Industry of Japan.