B－3－3 P-Column Gate Field Effect Transistor

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A new structure for a GaAs J-FET (P-Column Gate FET) is proposed, employing p-type column shaped gates in an active n-layer on a semi-insulating substrate where the current flows through channel spaces between the gate columns with results of 17 mS of g_m for prototype.

Figure 1 shows a microphotograph of and cross-sectional view of proposed P-Column FET. The channel is mainly controlled by depletion layers extending laterally from the columns at both sides of each channel and the columns completely reach the semi-insulating i-layer. It should be noted that the channel can be confined within n-layer near the n-i interface because of junction contour curves inward since the n-dopants decrease towards the i-layer. Moreover, MIS structure at the gate electrode metal on insulator/n-layer enables additional gate action. The gate pinch off voltage is predominantly determined by column sidewall distances and is controllable with lithography independently on n-layer thickness. Be ion implantation[(1)] was carried out through the lithography resist with windows corresponding to the P-Columns to be formed. The typical parameters are as follows.

Energy: 100 keV, Dose: $5\times10^{14}cm^{-2}$, Projected Range: 0.28 μm, Lateral Spreading of Be: 0.87 μm, Annealing Temp./Time: 600 °C/20 min., N-layer Thickness/Density: 0.18 μm/$2.8\times10^{17}cm^{-3}$.

Figure 2 shows an example of I-V curves for FET fabricated with 2 μm window size which results in ~3.7 μm P-Column diameter due to the lateral stretch of the implanted Be by 100 keV. No hysterisis on I-V was observed despite of the buffer-less n-layer on bulk i-substrate, presumably due to the channel confinement mentioned above. For 100 μm of equivalent gate width (n-channel number×n-layer thickness×2), was obtained 17 mS of transconductance being higher than in case of ordinary MESFETs with the same 100 μm gate width. Gate action in P-Column FET is made by two kinds of depletion swing, i.e. one at the column side walls and the other at the MIS surface structure. The MIS partition on g_m has linear dependence on n-surface length along the column lines but the column side wall partition on g_m has none on that length. Thus Fig.3 implies g_m is sustained by combination of the above both partition, disclosing a merit of P-Column structure.

Column spaces vs I_{DSS} (per 100 μm equivalent gate width) is plotted in Fig.4, where horizontal axis is the interspaces between 2 μm column windows. Linearity shown here between the interspace and I_{DSS} verifies that photolithographic controll of the interspaces between the columns can determine the pinch off voltage regardless of n-layer thickness, namely normally-off FETs for logic is easily realized by the column structure without n-layer thickness controll.

Estimated $f_T(=g_m/2\pi C_{GS})$ from measured g_m and C_{GS} is about 3 GHz for the column diameter of 3.7 μm fabricated as the first trial. Assuming $g_m \propto (\text{column diameter})^{-1}$ and $C_{GS} \propto (\text{column diameter})$, f_T is improved to about 30 GHz by realizable column diameter of about 1 μm which is possi-

ble by less lateral stretch of Be with lower energy (e.g. 30 keV) implantation and 0.5 μm column window size of resist utilizing electron beam lithography.

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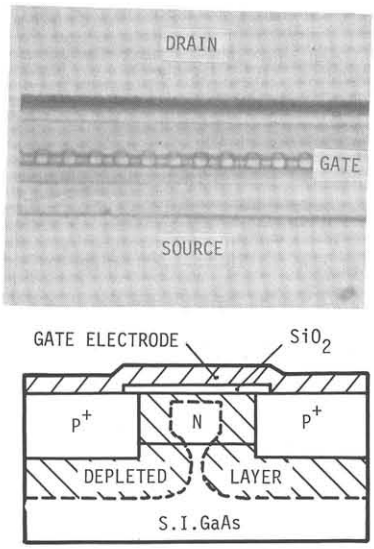

Fig.1 Structure of P-Column FET
(a) Plan View: Distance between source and drain is 8 μm. Column window size and the interval are 2 μm both.
(b) Cross-sectional View: P-type regions laterally spread from the window of mask by about 0.87 μm. Broken line is depletion edge at P-N junction and also by surface MIS effect.

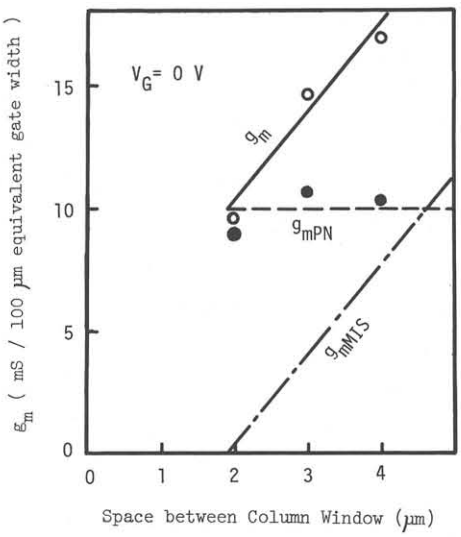

Fig.3 "g_m" Dependence on Column Spaces
"g_m" is normalized by 100 μm equivalent gate width. $g_m = g_{mPN} + g_{mMIS}$, equivalent gate width = (number of n-channel between total columns) × (thickness of n-layer) × 2

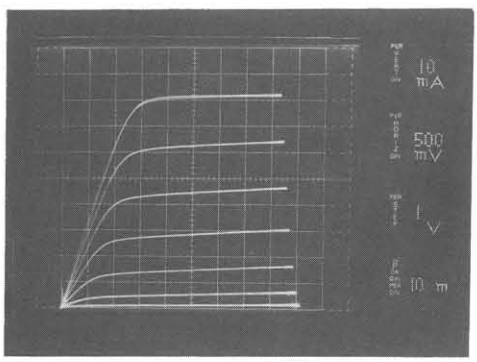

Fig.2 Typical I-V Curves of P-Column FET
(I_{DSS}= 82 mA, V_{pinch}= -6 V)

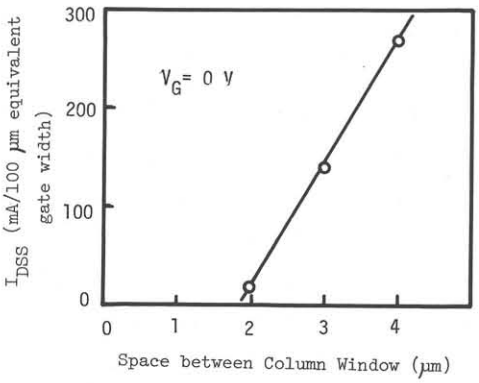

Fig.4 I_{DSS} Dependence on Column Spaces
I_{DSS} is normalized by the 100 μm equivalent gate width as in case of Fig.3.