B－3－6 Effect of Long Term Stress on Hot Electron Trapping

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In order to maintain the device reliability on VLSI, the hot electron emission and trapping characteristics must be carefully analyzed. So far the hot electron trapping has been understood in the following approach with the relationship of substrate current I_B, gate current I_G and gate-to-source voltage V_{GS}. Figure 1 shows I_B and I_G versus V_{GS}. With increasing gate bias, the I_B has a peak. This behavior can be explained by the two effects, that is, the increase in the channel current and the reduction in multiplication factor of the impact ionization with increasing gate bias. On the other hand, the gate current I_G is not appreciable in the region of V_{GS} smaller than V_{DS}. Indeed, as expected from the mentioned description, the I_G begins to be observed for $V_{GS} \geqq V_{DS}$, although the I_G decrease again as the IGFET goes further into the impact ionization does not occur. So far the worst gate bias condition for the hot electron trapping has been considered to be $V_{GS} \geqq V_{DS}$ which gives enhanced gate current. However, if the effects of the gate bias on the threshold voltage shift are examined under long term stresses, more remarkable trapping effects can be found under $V_{GS} < V_{DS}$ rather than $V_{GS} \geqq V_{DS}$. This work presents the hot electron trapping characteristics which is described for the long term device degradation.

The measured IGFETs had silicon gates and were fabricated on ⟨100⟩ p-type 20 Ωcm silicon substrate. To control the threshold voltage, boron was implanted with the dose of $2 \times 10^{11}/cm^2$. The junction depth of source and drain was 1μm. Devices were stressed in the dark at 30°C. The threshold voltage were measured when the drain current equals 1μA at V_{DS}=0.1V and substrate bias V_{sub}=-5V.

Figure 2 shows the effect of the gate bias on the threshold voltage shift ΔV_{TH} of IGFET. The threshold voltage shifts increase with time and decreasing gate bias. It should be noted that the time dependence on the rate of V_{TH} shift is consistent with the V_{GS} dependence since the electron trapping in the gate insulator has the same effect as the decrease in the gate bias. Figure 3 shows the rate of the V_{TH} shift R_{VS}, which is defined as the inverse time at ΔV_{TH} =30mV shown in figure 2, the substrate current, and the gate current as a function of the gate bias. The threshold voltage shift has a mutual relation not with the gate current but with the substrate current. Figure 4 shows the

gate bias dependence of R_{VS}/I_B as a function of the gate insulator thickness. From this figure, it is found that R_{VS}/I_B increases with decreasing V_{GS}. Therefore, this gate bias effect can not be explained by only the substrate current which corresponds to the total amount of the secondary hot electrons. Figure 5 which is obtained by transforming figure 4 shows that R_{VS} depend on only the electric field in the gate insulator, and that R_{VS} becomes larger with the reduction of electric field in the gate insulator. All the data show that the large amount of hot electrons are injected into the gate insulator even if V_{GS} V_{DS} and that the trapping efficiency increases with the repulsive electric field in the gate insulator. In other word, by the larger repulsive field in the gate insulator, the injected hot electrons can stay longer in the insulator and so the trapping efficiency becomes larger. The relationships of degradation between IGFETs and actual MOS dynamic memory will be also discussed.

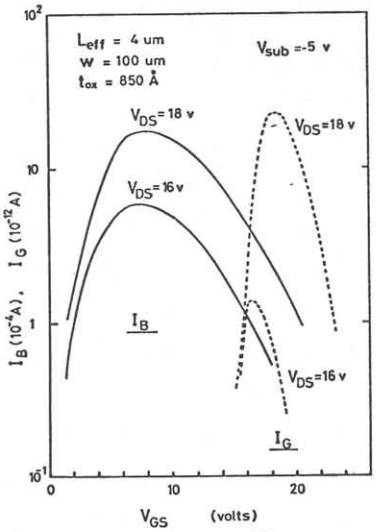

Fig. 1 I_B and I_G vs. V_{GS}

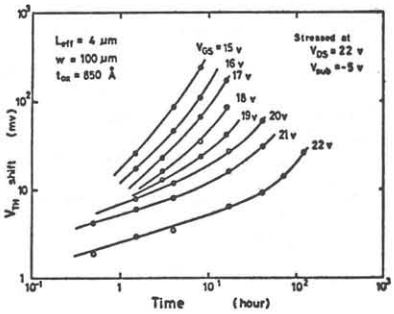

Fig. 2
V_{TH} shift vs. time

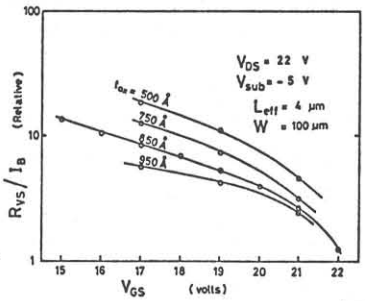

Fig. 4
R_{VS}/I_B vs. V_{GS}

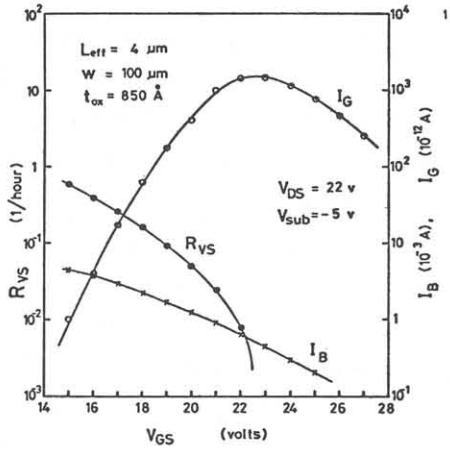

Fig. 3 R_{VS} vs. V_{GS}

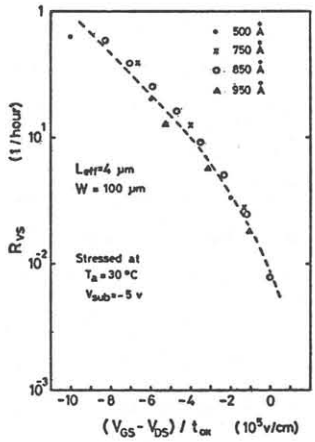

Fig. 5
R_{VS} vs. electric field in the gate insulator