C－4－4 An Improved Josephson Interferometer Memory Cell for Nondestructive Read-Out

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Single flux quantum (SFQ) Josephson interferometer memory cells have already been studied experimentally.[1-2] However, thus far tested SFQ memory cells have been restricted to destructive read-out operation. A nondestructive read-out (NDRO) SFQ interferometer memory cell has been proposed by Beha[3], which is constructed with a center-fed two-junction interferometer having unequal junction size. The proposed NDRO operation is based on reading of the mode N=0 by a vortex-to-voltage transition which is followed by a stable return to the mode N=0 after switching off the operating currents. The current trajectory for NDRO operation should cross the vortex mode boundary far above the critical point which defines the critical interferometer current for a vortex-to-voltage transition. In Beha's configuration, however, the current trajectory was selected so as to cross the mode boundary having a higher critical point[4], which caused the redused bit operating current margin.

In this paper, we propose an improved NDRO-SFQ interferometer memory cell bringing about the wide bit operating current margin, in which the current trajectory for NDRO is selected so as to cross the mode boundary having a lower critical point.[4] For this current trajectory, the zero field threshold current $I_m(0)$ of the mode N=1 restricts the bit operating current to a low level in the case of the center-fed asymmetric interferometer. To exclude this restriction, the present cell was constructed with the end-fed asymmetric two-junction interferometer, the equivalent circuit of which is shown in Fig.1(a), $LI_{ji} = \Phi_0$, L=1.0 pH and I_{j2}/I_{j1}= 3.3 (where $\Phi_0 = 2.07 \times 10^{-15}$ Wb is one flux quantum).

In Fig.1(b) the calculated threshold curve of the present cell is shown together with the critical points determined by computer simulations. The current trajectory for the memory operation is also shown in Fig.1(b). The NDRO operation and writing of a "1" (the mode N=0) are carried out by a vortex-to-voltage transition, while writing of a "0" (the mode N=1) is carried out by a vortex-to-vortex transition.

The dynamic condition for proper memory operation is important in this type of the memory cell. The required range of the McCumber damping parametr $\beta_c = (2\pi/\Phi_0) I_j C R_{SG}^2$ (where I_j is the maximum Josephson current, C the capacitance and R_{SG} the subgap tunneling resistance) was determined by computer simulations for 100 ps rise and fall times of the operating currents. The obtained values of β_c was from 250 to 450.

The experimental device fabricated and tested was a 2 x 2 bit memory cell

array. A SEM micrograph of the cell is shown in Fig.2. The device was fabricated by means of 10μm standard Josephson technology[5] for 1 kA/cm^2 Josephson current density. In order to obtain β_c values from 250 to 450, In-content of the base-electrode was selected as 8 wt%, which gave the optimum subgap- to normal- tunnelig resistance ratio, R_{SG}/R_{NN} = 3~4.

Basic memory operation was experimentally confirmed at a 100 kHz repetition rate. A write-read sequence with write "1" - three cycles repeated read "1" - write "0" - three cycles repeated read "0" is demonstrated in Fig.3, which shows the proper write and NDRO operation. The tolerances of the operating currents restricted by the thresholed curve were ± 9% for I_{bit} and ±11% for I_{word} and I_{write}. The operating region of I_{bit} was fully effective because the bit operating current level was set far above the critical point.

In conclusion, we have described the improved NDRO-SFQ interferometer memory cell. The stable NDRO operation with wide margin was successfully obtained.

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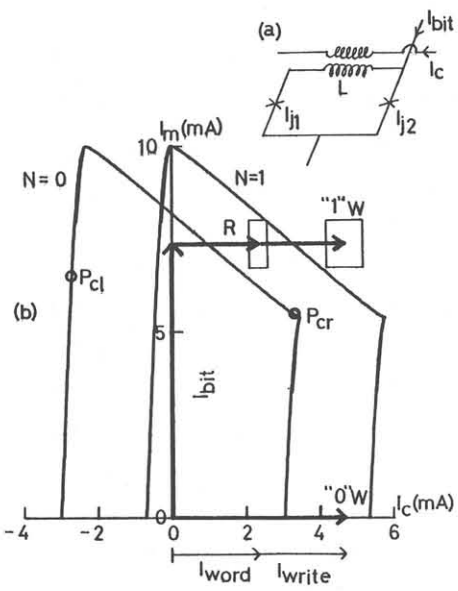

Fig.1 (a) The equivalent circuit of the present cell. (b) The calculated threshold curve and the computer simulated critical points P_{cr} and P_{cl}.

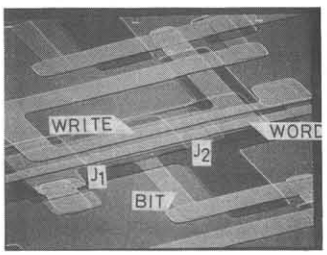

Fig.2 A SEM micrograph of a fabricated memory cell.

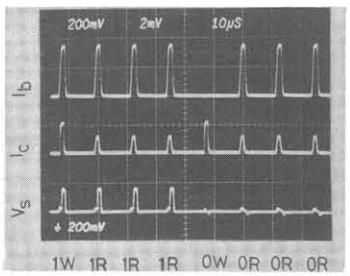

Fig.3 A write-read sequence. The sense voltage V_s (2mV/D), the control current I_c (4mA/D) and the bit current I_{bit} (4mA/D).