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C-4-5 A Two-Josephson-Junction Memory Cell with Nondestructive Readout

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Many types of NDRO Josephson memory cell have been investigated and developed.[1)-4)] They are divided into two groups. One is a memory cell with an insulated sense gate which is part of an interrogate line.[1),2)] Therefore its structure is rather complex. The other is a single flux quantum NDRO memory cell with no sense gate. The NDRO operation is achieved by the asymmetric structure and the strong damping of the memory loop.[3),4)] And it requires a diagonal line in addition to X and Y lines.

A comparably simple NDRO Josephson memory cell has been proposed and tested. This cell with no sense gate consists of a planar superconducting loop with two Josephson junctions, a word line, a control line and a data line. Information can be stored in the memory loop with no bias current.

The equivalent circuit of this memory cell is shown in Fig. 1. The memory loop stores a persistent circulating current in the "1" state, or no current in the "0" state. The vertical word line A interconnects all memory loops of a column serially, and the horizontal control line B runs throughout a memory array. The control current I_b on line B decreases the critical current of each junction, however, does not make an inductive coupling with memory loop because the line divides the loop into two equal area. The horizontal data line C couples with the memory loop inductively.

In Fig. 2 is shown the threshold characteristics of this memory cell. The right and left of the abscissa represent the value of the data current I_c and the value of the control current I_b respectively. The ordinate represents the word current I_a. The upper and the lower curves "0" are I_a-I_c curves with I_b=0 and that with I_b=I_B respectively. When the persistent circulating current corresponding to a "1" is stored in the loop, the I_a-I_c curves are shifted like the upper curve "1" (I_b=0) or the lower curve "1" (I_b=I_B).

Writing information into the memory cell is accomplished by the coincident application of I_a=I_A, I_b=I_B and the data signal on the line C. The coincidence of I_A and I_B switches both junctions into the voltage state independent of stored information. The application of the data signal I_c=I_W and subsequent removal of I_A and afterwards I_W make the persistent current in the loop (writing "1"). The same sequence with I_c=0 makes no circulating current (writing "0").

Readout operation is performed by the coincident application of $I_a=I_A$ and $I_c=I_R$. If a "1" has been stored, the memory loop stays in the zero-voltage state (operating point is under the upper I_a-I_c curve "1"), and the sensing voltage V_a is zero. If a "0" has been stored, the loop switches into the voltage state (operating point is over the upper I_a-I_c curve "0"), and the sensing voltage V_a occurs. NDRO operation is achieved by first removal of I_R and subsequent removal of I_A. The memory loop returns to the zero-voltage state with no circulating current for the "0" state.

In this memory loop the number of flux quanta in the "0" state may fluctuate around 0, however in the "1" state (the memory loop stores magnetic flux $n\Phi_o$) n is about 100, so it is easy to distinguish the "1" state from the "0" state.

Fig. 3 is a microphotograph of the memory cell. Pb-Au-In and Pb-Au alloys are used to form the Josephson junctions.

In Fig. 2 bars indicated as I represent the experimental results of a threshold curve and bars indicated as represent the operational margin of the memory cell.

References

1) W. H. Henkels and H. H. Zappe, IEEE J. Solid-State Circuit, SC-13, 591,(1978)

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3) H. Beha, Electronics Letters, 13, 596, (1977)

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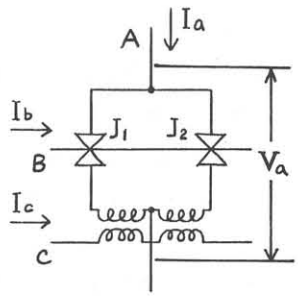

Fig. 1. Equivalent circuit of the memory cell

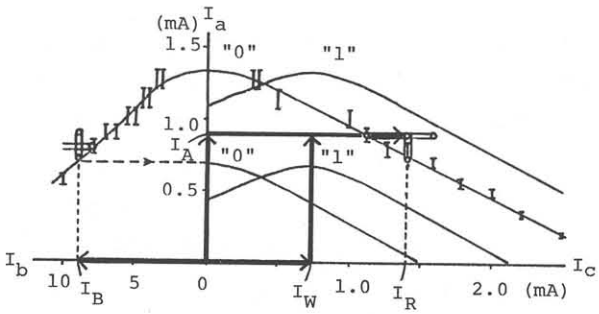

Fig. 2. Threshold curves and driving pulses of the memory cell

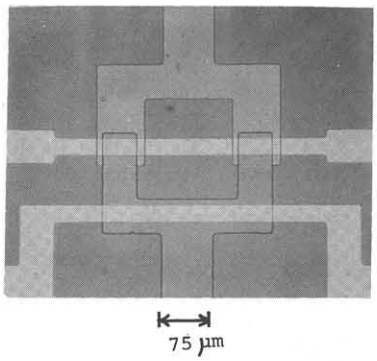

Fig. 3. Microphotograph of the memory cell