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A Potential of Bipolar VLSI

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1. Introduction Bipolar devices have been thought of as devices for high speed integrated circuits, while MOSFETs are the devices for VLSIs. In this talk I will discuss the possibility of using bipolar devices for high density VLSIs.

2. Some Fundamental Limitations In general, the integration level, N_G (gates/chip), and speed, t_{pd} (delay/gate), of an integrated circuit have the following fundamental limitation:

$$\frac{N_G}{t_{pd}} \leqq \frac{\Delta T}{\theta E} \qquad (1)$$

where ΔT is the allowable temperature difference between at the pn junction of the device to the ambient temperature ($\Delta T=T_j-T_a$), θ is the thermal resistance between the pn junction and the ambience, and E is the switching energy per gate. It is clear that, for a high performance VLSI, $\Delta T/\theta E$ should be as large as possible. There is little difference in ΔT and θ between bipolar or MOS VLSIs, while values of E depend upon device structures and circuit configurations. It should be noted that ΔT, θ and E have equal importance in the performance of VLSI.

If we take typical values of $\Delta T=100°C$, $\theta=25°C/W$, and E=1pJ for the bipolar and 0.25pJ for the MOS, then

$N_G/t_{pd} \leqq$ 4,000 (gates/ns) for bipolar or $\leqq$ 16,000 (gates/ns) for MOS.

As shown in Fig.1, the maximum integration level of a high speed (tpd=0.5ns) bipolar LSI is 2,000 gates/chip, while that of a typical MOS VLSI (tpd=5ns) is 80,000 gates/chip. Bipolar has been far behind MOS in this respect.

3. Switching Energy Let's investigate the switching energy, E, in more detail. It is the product of the power dissipation per gate, P_d, and the switching time, t_{pd}. In most cases E is given by $E=P_d \cdot t_{pd}=k_d \cdot CV_l V_s$ (2), where k_d is duty ratio, C is average loading capacity for a gate, V_l is logic swing and V_s is supply voltage for the gate. k_d depends upon circuit configuration, and is the order of 1/2 for a static circuit and much less than 1/10 for a dynamic circuit or a CMOS circuit. Here, MOS has salient advantage over bipolar. C depends upon the geometry of the device and the wiring structure. It seems that there is no essential difference between bipolar and MOS in this respect. V_l and V_s depend upon how the device operates at low voltage, how the device controls its output current with a minimum change of input voltage and how strong is the non-linearity of the device. It is in this respect that bipolar surpasses MOS. The bipolar transistor has a low threshold voltage of $V_{be}=0.6V$.

It has a large transconductance, and also has non-linearity of the form exp(qV/kT). The collector current can be controlled one order of magnitude by a base voltage of 2.3kT/q, or 60mV.

4. I^2L Circuit The cicuit with the lowest supply voltage would be the I^2L circuit, which is shown in Fig.2. Note that only one diode-voltage, 0.7V, is required for V_s. Theoretically, this circuit can switch the output current if $V_s > kT/q$. The possible minimum supply voltage could be as low as $10kT/q = 0.25V$. If we take, for example, $k_d = 1/2$, $V_l = 0.5V$, $V_s = 0.6V$, then $E = 0.15C = 0.15$ (pJ/pF). This means that, even with 1pF loading capacitance, the E value for this I^2L circuit is better than the MOS circuits mentioned above.

Recently, highly self-aligned I^2L structures that would allow effective scale down with minimum loading capacitor have been proposed[1), 2)]. It has also been shown, by computer simulation, that a scaled down I^2L will have a switching speed of 150ps when its collector size is 0.5μm[3)].

5. A Hypothetic Bipolar VLSI Suppose one-micron technology is available for bipolar as well as for MOS. Also assume a conservative value of C=0.5pF. Then we get

$$N_G/t_{pd} \leqq 53{,}300 \text{ (gates/ns)}.$$

Thus a 80 k-gate VLSI with $t_{pd} = 1.5$ns will not be impossible. Such a bipolar VLSI could compete favorably with a MOS VLSI in density as well as in performance.

6. Premiums for Bipolar VLSI Furthermore, future VLSI should have the capability of analog functions on the same chip. Sensitive amplifiers and powerful power devices are certainly premiums for bipolar VLSI.

1) D.D.Tang et al., IEEE Trans. Electron Device, ED-27, p.1379, 1980

2) T.Nakamura et al., IEEE ISSCC Digest of Technical Papers, p.214, 1981

3) Y.Okada et al., Annual Meeting of IECS of Japan, No.352, 1981

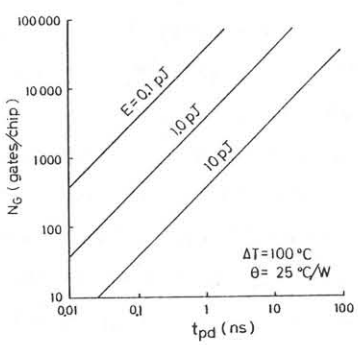

Fig.1 Maximum integration level as a function of delay time

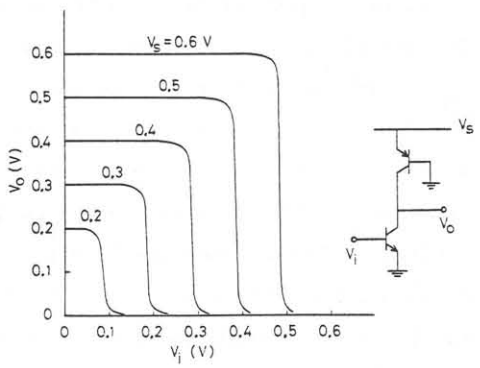

Fig.2 Transfer characteristics of I^2L