A-1-2 A High-speed I^2L Process / Structure for VLSI

T. Hirao, H. Ishikura, S. Ohsaki and N. Tsubouchi
LSI R&D Laboratory, Mitsubishi Electric Corporation
4-1 Mizuhara, Itami 664 Japan

A high-speed I^2L gate for VLSI applications has been successfully designed, characterized and demonstrated. The high speed performance has been achieved in an oxide isolated I^2L with a buried base structure by means of a thin epi-layer and heavily doped extrinsic base, and characterized by 0.87 ns of minimum gate delay (t_{pdmin}) at fan-out (F.O.) =1 and 1.5 ns at F.O.=3. The I^2L characteristics have been superiorly controlled by optimizing the impurity profile with the reduced pressure epitaxy. The influence of device structure on the gate speed has been investigated and then the typical performance for the high speed gate-array VLSI which allows gate speed down to 3.7 ns (F.O.=5) at 0.45 mW/gate power-dissipation has been obtained with the high packing density of 700 gates/mm^2 in 3.4 μm design rule by a dual injector structure and this optimized process.

A. PROCESS Fig.1 shows the cross-sectional view of a buried base I^2L gate with the oxide isolation. The buried base I^2L with the arsenic (As) buried emitter resulted in higher speed than that with the antimony (Sb) buried emitter, as shown in Table 1[1]. However, the deviation of β_u in the As buried emitter I^2L was approximately 16 % in the run-to-run production, which was limited by the base width variation. In the case of the reduced pressure epitaxy, the impurity concentration of the intrinsic base region was lower and the base width was wider than that with the conventional atmospheric pressure epitaxy, respectively.
The deviation of β_u in the As buried emitter I^2L with the reduced pressure epitaxy was found to be about a half of that with the conventioanl epitaxy.
Fig.2 shows that the I^2L gate speed depends on the epi-layer thickness and the extrinsic base resistance. As a result of thin epi-layer and heavily doped extrinsic base, the t_{pdmin} has been reduced to a half value of that without optimized process parameter, as shown in Table 1.

B. STRUCTURE At higher currents the base resistance was more important for I^2L gate speed. The t_{pdmin} decreases with decreasing the distance between the collector and base contact (D_{C-B}) as well as the extrinsic base resistance, as shown in Fig.2, because of the reduction of the base resistance. Fig.3 shows the t_{pdmin} of the various fan-out I^2L gates versus the collector-emitter breakdowen voltage (BV_{CEO}) of upward switching transistor. As the BV_{CEO} decreases, the β_u becomes higher and then the I^2L gate speed is improved. In the case of the dual injector structure illustrated in Fig.1, the I^2L gate speed with F.O.=5 was led to be almost the same value (t_{pdmin}=2.3 ns at BV_{CEO}=1.0 V) as that of the single injector I^2L

gate with F.O.=4 due to the small base resistance, as shown in Fig.3 by the dashed line. Furthermore, the contribution of the scaled process to the speed performance is shown in Fig.2, which is different from the conventional I^2L gate[2] with saturation of the scaling effect. In consequence of scaling down to 2.5 μm design rule (minimum contact ; 1.5 X 2.5 μm^2), 10K gates array VLSI would be fabricated with the average propagation delay of 2.5 ns at 0.26 mW/gate and high packing density of 2.4 mm□/10K-gates.

A high-speed performance I^2L for VLSI has been accomplished by a dual injector and buried base structure with the reduced pressure epitaxy technology.

1) T. Hirao, et al : 12th Conf. on Solid State Devices, Tokyo, 1980, Jpn. J. Appl. Phys. 20 (1981) Suppl. 20-1.

2) S.T. Evans :IEEE J. Solid-State Circuits SC-14 (1979) 318.

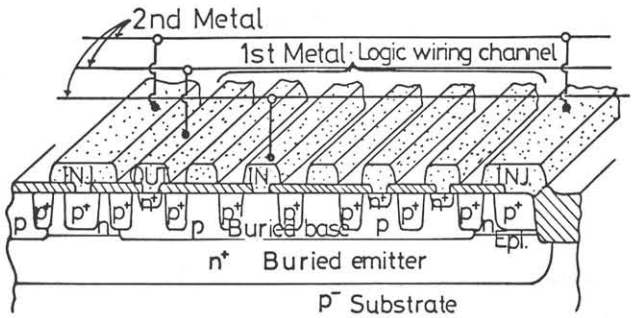

Fig.1 Schematic structure of dual injector I^2L with buried base structure for gate-array VLSI.

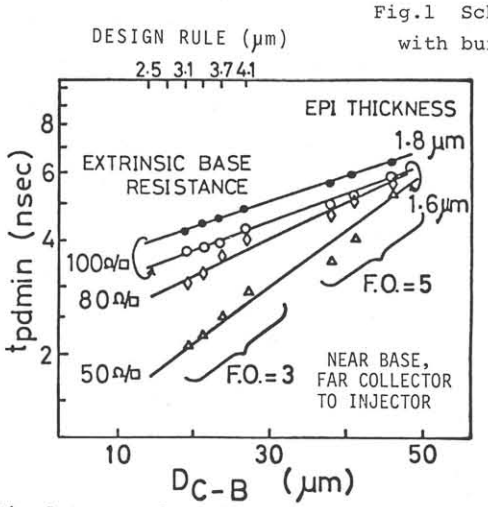

Fig.2 t_{pdmin} dependence on the collector and base contact (D_{C-B}).

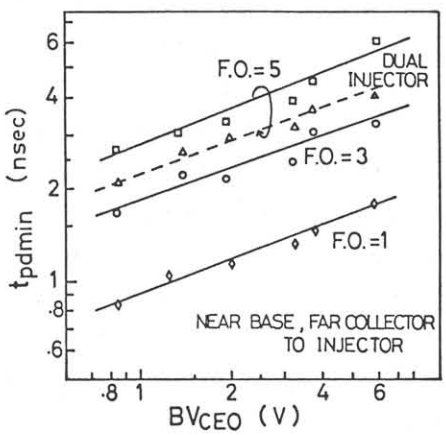

Fig.3 t_{pdmin} of the various fan-out I^2L gates versus BV_{CEO} of upward switching transistor.

Table 1. Device performances in a buried base I^2L gates.

Buried emitter impurity	Sb	AS	AS	AS
Epitaxical growth condition	SiH_4, 760 Torr		SiH_2Cl_2, Reduced pressure	
Epi-layer thickness	1.8 μm	1.8 μm	1.8 μm	1.6 μm
Extrinisic base resistance	100 Ω/□	100 Ω/□	100 Ω/□	50 Ω/□
Minimum delay time	5.2 ns	4.2 ns	4.3 ns	2.5 ns
Power-delay product (I_{inj}=1uA)	45 fJ	65 fJ	47 fJ	93 fJ
Standard deviation of β_u	11.5 %	16.7 %	8.9 %	—

Design rule ; 3.7 μm (minimum contact size ; 3.0X3.0 μm^2). Ring oscillators have a near base, far collector with 3 collectors (F.O.=3), all with respect to a injector.