

A-1-3 Quasi-Three-Dimensional Approach to Transient Analysis of  $I^2L$  Devices

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I. Introduction

In order to improve the speed of  $I^2L$  devices, it is necessary to understand perfectly the transient behaviour at high injection levels. The importance of high injection effects, and two-dimensional and three-dimensional effects on minimum delay time has been pointed out [1]-[3]. However, applying exact three-dimensional numerical analysis procedures to the transient characteristics is extremely difficult because of the requirement of enormous computational time.

Quasi-Three-Dimensional (Q3D) modeling, as was originally proposed by Engl et al [4], describes the three-dimensional device as a network of partitioned device units, each of which can be analyzed by one-dimensional model. This method has the merits of sufficient accuracy within a reasonable computational time and obtaining directly the guide for improving device structures. The present authors have recently analyzed  $I^2L$  devices in DC and AC states starting from their doping profiles and layout patterns, and the results are in good agreement with the measured ones [5].

In the present work, we extend the theory to the transient analysis of  $I^2L$  devices. A comparison is made between the computation and the measurement. Thus we have established quantitatively the effect of lateral voltage drop on the delay time of  $I^2L$  devices.

II Analysis and Comparison with the Experiments

The sectional view of a single collector  $I^2L$  device with conventional structure is shown in Fig.1(a). The dotted lines in Fig.1(b) indicate partitioning planes. The partitioned units are lateral transistor (LT) units, vertical diode (VD) units, and vertical transistor (VT) units. For the present calculation the number of units is 21 per gate. The VD and VT units are one-dimensional units, and LT units are modified-one-dimensional units, where the dependence of area and volume on the position is added to simple one-dimensional model [6].

The delay time is estimated by calculating the transient behaviour of 4-stage cascade of  $I^2L$  inverters (see Fig.2(a)), and is checked with the measured data of a 11-stage ring oscillator. The theoretical delay time is half of  $2\tau_d$  in Fig.2(b). By using a HITACHI M-200H computer (8-10 MIPS), typical computational time is 5-10 sec per transient state for the circuit containing about 80 units.

Figure 3 shows injector-current dependence of delay time. The computed results (solid line) agree very well with the measured ones (open circles) even at high current levels.

If all the effective resistances connecting the adjacent units are assumed to be zero, that

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is, lateral voltage drop in DC state (position dependence of stored charge) and in transient state (charging or discharging through base resistances) is neglected, the computed results change as the broken line of Fig.3, although the high injection effects are still retained in the model. An improvement on delay time by a factor of 2 is expected if the lateral voltage drop can be totally eliminated.

### III Conclusion

A high-accuracy Quasi-Three-Dimensional modeling of  $I^2L$  devices in transient analysis is developed. Delay time at high current levels is strongly affected by lateral voltage drop even for a single collector  $I^2L$  device with conventional structure. If lateral voltage drop is reduced, for example by using a metal base structure, the delay time at high current levels is predicted to be improved by a factor of 2. The present method of analysis is equally applicable to the improved features such as self-aligned  $I^2L$  or the structures with upward base internal field.

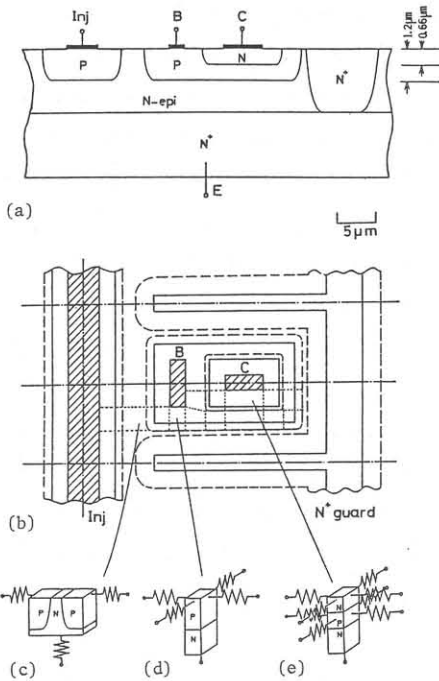


Fig.1 Configuration of  $I^2L$  device and its Quasi-Three-Dimensional model: (a) cross section, (b) top view and partitioning planes (dotted lines), (c) LT unit, (d) VD unit, (e) VT unit.

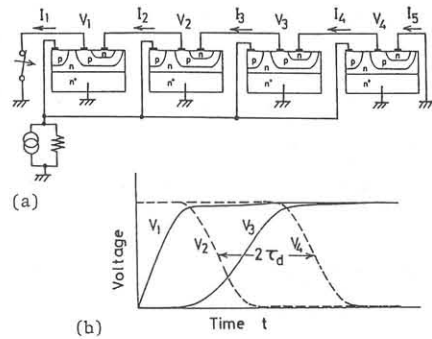


Fig.2 Estimation of delay time. The switch is turned off at  $t=0$ .

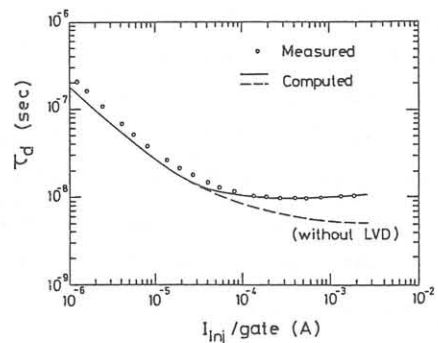


Fig.3 Injector-current dependence of delay time.

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