Digest of Tech. Papers The 13th Conf. on Solid State Devices. Tokyo

A-1-4

U-groove Isolation Technology for High Density Bipolar LSI's

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The area of active regions in bipolar LSI's is now decreasing due to advances in fine lithography. However, when using conventional oxide isolation, reduction of the inactive isolation region is limited by the 'bird's beak' and isolation voltage. Therefore, a new isolation technology which allows significant reduction in isolation area through using U-grooves filled with oxide and polysilicon has been developed. This U-groove isolation (U-Iso) technology has realized a minimum isolation distance of less than 3 µm.

A cross-sectional view of the U-Iso is shown in Fig.1, together with that for conventional oxide isolation. U-grooves (Y-shaped grooves) are formed by anisotropic etching and a reactive sputter etching of silicon. The slope of the upper part of the grooves is provided to avoid the surface steps. The grooves are then oxidized and covered with Si_3N_4 film. Polysilicon film with a thickness equal to the depth of the groove is deposited on the wafer, and then selectively etched so it will have a flat surface, by using a conventional photo-etching technique. Finally, the surface of the polysilicon is oxidized to make a passivation layer. A SEM micrograph of the cross section of U-Iso is shown in Fig.2.

Isolation characteristics for U-Iso are shown in Table 1. It is known that the isolation distance of conventional oxide isolation is limited by the length of the 'bird's beak', the isolation voltage, and the accuracy of mask-alignment. On the contrary, the distance for U-Iso is determined by only the width of the isolation groove. Therefore, it can be understood from Fig.1 that the minimum isolation distances are 3 µm, and 7 µm, for U-Iso, and conventional oxide isolation, respectively. Device sizes can also be cut down, due to the reduction of the isolation area. For example, transistor size for U-Iso is 189 μm^2, whereas that for conventional oxide isolation is 435 μm^2.

Isolation voltage (BV_{CCO}) and isolation capacitance (C_{TS}) are also improved to a great extent. As neighboring N^+ buried layers are separated by a deep U-groove, the P^+ channel stop layer formed by B ion implantation is out of contact with the buried layers. Therefore, the breakdown voltage between the N^+ buried layer and the substrate (BV_{CSO}), and the punch-through voltage between the neighboring N^+ buried layers increase, and the peripheral component of the isolation capacitance ($C_{TS\ell}$) decreases drastically.

Figure 3 shows the relationship between isolation voltage and isolation distance. The Xs and dashed lines respectively indicate the experimental data and the theoretical value calculated from a simple model. This figure shows that the U-Iso isolation voltage remains high for various isolation distances.

In order to confirm the practicability of the U-Iso technology, ECL integrated circuits were fabricated. Figure 4 shows a SEM micrograph for an 11-stage ring-oscillator. Measured propagation delay time was 0.39 nS/gate. Transistor characteristics were as good as those for a conventional oxide-isolated transistor.

In conclusion, U-Iso technology can be successfully used for fabricating high density bipolar LSI's. This technology allows a small isolation distance, high isolation voltage, low isolation capacitance, and 60% reduction in transistor area.

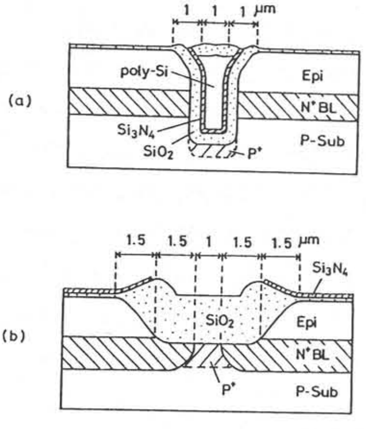

Fig.1 Cross sectional structure for U-Iso (a) and conventional oxide isolation (b)

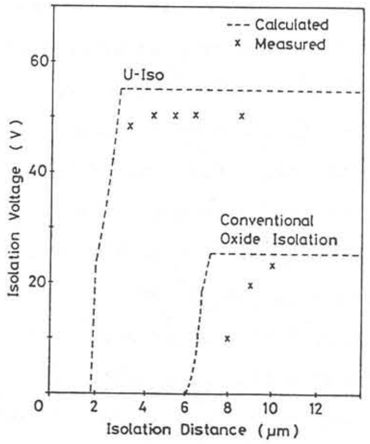

Fig.3 Comparison of Isolation voltage

Table 1. Isolation Characteristics

	U-Iso	Conventional Oxide Isolation
Minimum Isolation(µm) Distance	3	7
Isolation Voltage (V)	50	25
Isolation Capacitance(pF)	0.02	0.1
Transistor Size (μm^2)	189	435
Surface Steps	gentle	steep

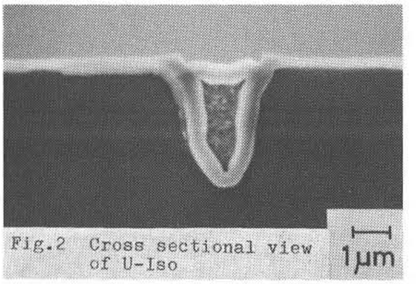

Fig.2 Cross sectional view of U-Iso

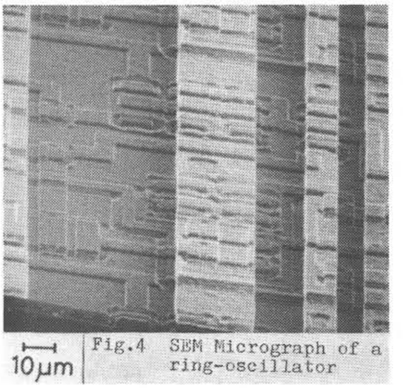

Fig.4 SEM Micrograph of a ring-oscillator