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VLSI Fine Technology and Its Problems

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VLSI fabrication technology with minimum pattern dimension below 1 μm is not necessarily an extension of technology practiced for larger pattern dimension. It requires a new viewpoint and novel approarches. In this report we review the approarches to 1 μm 256K MOS RAM process and problems encounterd in the process development[1-4].

Guiding principles of the 256K development were miniaturization based upon the scaling-down law, reduction of interconnection resistance deviating from the law, and introduction of fault-tolerant technology to meet yield reduction[1]. Major processing technologies developed are electron beam direct writing[3] and dry etching[4] for 1 μm pattern formation with ± 0.1 μm width accuracy, Mo gate technology[2] for interconnection with lower resistivity than that of polysilicon, and fault-tolerant circuit with electrically programmable PROM[1]. Minimum linewidth at various writing levels and device parameters of the 256K are listed in TableI.

On the way of 1 μm process development, many problems inherent in above technologies have been found out, in which some problems have not been reported so far. These problems are summarized in Table II and some examples are explained in the followings. A defect caused by the collected stress at the Si_3N_4 mask pattern edge during selective oxidation is shown in Fig.1, where the defect is observed after removal of Si_3N_4 film by plasma etching[5]. This phenomenon means that the stress at the pattern edge sharply defined by EB lithography is so strong as to cause crack of the film. In contact hole etching, columnar residues are observed for high H_2 content in CF_4+ H_2 reactive gas mixture, which is shown in Fig.2. The residues are caused by plasma polymerization and degrade the contact resistance[4]. Mo film properties such as step coverage, mobile ion contamination, adhesion to SiO_2 and masking ability against ion implantation are strongly dependent upon the deposition methods, i.e., EB evaporation, RF sputtering and CVD, while the grain size and nitridation of Mo mainly depend upon the temperature and ambient of heat treatment[6]. From the As distribution profile measurement in Mo film, it was confirmed that the masking ability of Mo decreases with increasing grain size and the degradation of the ability is caused by channeling phenomenon[7].

With increasing integration level in future, finer and more accurate

pattern delineation and thinner film with lower defect density will be required. To realize these finer technologies, it is important to develop not only processing technology but also evaluation technology with higher resolution. In addition, the device technology must be developed to overcome the decrease of breakdown voltage of gate oxide, junction and punchthrough, the increase of subthreshold leak of MOSFET, and the influence of hot electron and doping fluctuation[8].

References

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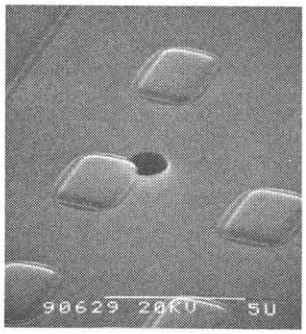

Fig.1. Defect generated at LOCOS pattern edge.

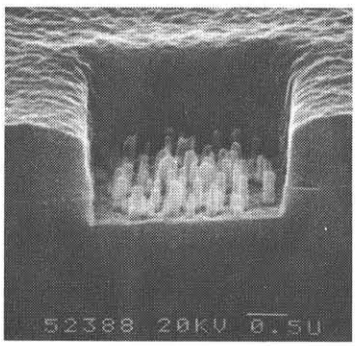

Fig.2. Columnar residues generated in contact hole.

Table I. Minimum linewidth at various writing levels and device parameters of the 256K.

Diffusion layer minimum linewidth	2.0 μm
Polysilicon minimum linewidth	1.1 μm
Molybdenum minimum linewidth	1.0 μm
Contact hole minimum dimension	1.0 μm square
Alminum minimum linewidth	1.1 μm
Gate oxide thickness	Si gate 30 nm, Mo gate 40 nm
n^+ junction depth	0.25 μm
Effective channel length	Si gate 1.2 μm, Mo gate 1.5 μm

Table II. Major problems encountered in the 1 μm process development.

Technologies	Problems
EB direct writing	Stress generated at the sharp pattern edge during selective oxidation. Radiation damage. Throughput.
Dry etching	Contact resistance·degradation caused by residues due to plasma polymerization. Junction degradation caused by damage and heavy metal contamination during etching.
Mo gate	Step coverage. Degradation of adhesion to SiO_2. Mobile ion contamination. Masking effect degradation against ion implantation.