

A - 2 -10 High Voltage Low On-Resistance VDMOS FET

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The power MOS FET is a promising device capable of handling high power at high frequency[1]. Recently, 0.3-0.4 ohm on-resistance devices with 400-500V sustaining voltage have appeared on the market[2]. However, their prices are still much higher than those of the corresponding bipolar devices.

This paper proposes a new technology to enable to obtain a low on-resistance vertical D-MOS FET at high manufacturing yield.

According to recent analysis on power MOS FETs[3], the most significant fraction of the on-resistance comes from the epi-layer, so that a low resistivity thin epi-layer is desirable. However, this contradicts concepts for high voltage design where a high resistivity thick layer is required. A good trade-off is achieved by introducing a new guard ring structure, as shown in Fig.1. This structure consists of a few guard rings, each of which has its own field plate. It was experimentally confirmed that the structure reveals excellent stability and realizes 90-100% of ideal flat junction breakdown voltage.

To show superiority of the new structure to conventional ones, histograms of attained breakdown voltages for three structures (conventional guard ring, field plate and the new structure) are compared in Fig.2. Samples were prepared on the same wafers in the same processes, with forming a 4-5 micron p^+ diffusion layer onto a 12 ohm-cm 38 micron epi-layer. In the new structure, 450-480V were easily obtained at more than 90% yield without any special care, whereas ideal breakdown voltage is around 480V in this case. One advantage of the new structure consists in that the layout for the inter-ring spacings is relatively noncritical in determining the junction breakdown characteristics, thus leading to high yield in actual device fabrication.

Another important problem is the optimum design for a source pattern. An exact two-dimensional numerical model[4] was developed for the problem. Calculations were carried out for simple stripe patterns. They assured that 0.07-0.08 ohm on-resistance per unit active area is easily obtained for 13 ohm-cm 40 micron n^- epi-layer with an optimized simple stripe pattern. Figure 3 shows calculation examples of on-resistance per unit active area vs. source to source distance L_G characteristics with source width L_S as a parameter. Detailed conditions and several experimental data are also shown in the figure. Agreement between theory and experiment is satisfactory. It is evident that narrow

source width and adequate source to source distance considerably improve device on-resistance.

The resistance in the completely accumulated channel is as low as 10% of the total on-resistance, so that the channel length and thus p^+ diffusion depth are not required to be so short or shallow.

On the basis of the above considerations, less than 0.24 ohm on-resistance with 450V breakdown voltage was easily obtained with a relatively wide 22 micron source width pattern and 6.5mm square chip.

For a commercial product, a 5.5mm square chip device was developed, using the source layer as lateral current paths so that 6 micron source width could be realized. Double p^+ and n^+ diffusions were performed using polysilicon DSA process. These made 0.35 ohm on-resistance device possible with a new guard ring structure. Other obtained characteristics are listed in Table 1.

REFERENCES

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- [4]. M.S. Mock, Solid-St Electron. 16, 601 (1973)

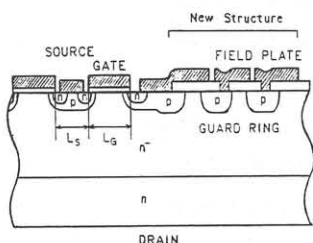


Fig.1 D-MOS Structure

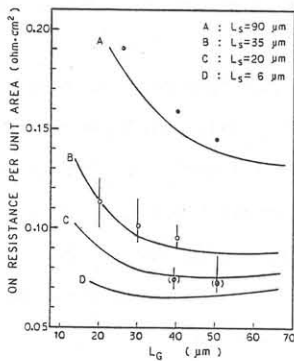


Fig.3 Unit Area On-Resistance
With a 5 μm p^+ Diffusion
Layer onto 13 ohm-cm 40
 μm Epi-Layer

Drain-Source Breakdown Voltage	450 V
Continuous Drain Current, I_D	10 A
On-Resistance ($I_D=5A, V_{GS}=10V$)	0.35 ohm
Reverse Transfer Capacitance ($V_{GS}=0, V_{DS}=10V, f=1MHz$)	70 pF
Forward Transfer Conductance	5-6 mho
Turn-On Time	120 nsec
Turn-Off Time	500 nsec

Table 1 Device Characteristics

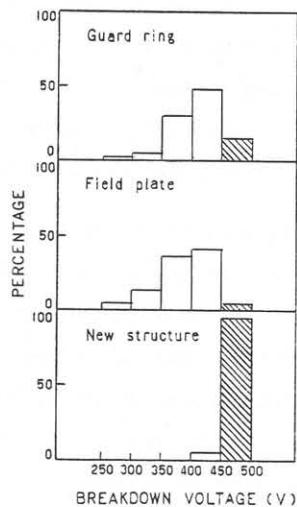


Fig.2 Histograms (about 50
samples for each)