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A－2－2 SOS CMOS 16 bit Parallel Multiplier

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As multiplication is essential in digital signal processing, many reports have been published on multiplier LSIs[1,2]. In this paper, a high performance 16 bit parallel multiplier is presented. It features SOS CMOS, which is suitable for logic LSI applications.

The multiplier configuration is shown in Fig.1, i.e., Full adder (F/A)+NOR cellular array. Device parameters and design rule outline are listed in Table 1. Although Si islands were formed by conventional anisotropic-etching method, gate-oxide break-down voltage is kept sufficiently high. Specially developed 1-D process-device[3] and 2-D device[4] simulators were utilized for fine pattern SOS MOSFET design, i.e., short-channel effect and back-channel leakage current suppressions. In circuit and mask pattern design, special design methods, due to SOS CMOS, can be used. "Sum" and "carry" circuits were designed separately, because of a high speed operation requirement (Fig.2). However, occupied area increase is relatively small. The n^+ or p^+ doped epitaxial Si layer is widely used as a signal line. This leads to higher packing density and less pattern design time without any additional parasitic capacitance. Parasitic capacitance, except at a line cross over point, can be ignored in circuit optimization process. F/A+NOR cell size is 230x190μm and chip size is 5.02x4.87mm. In order to evaluate multiplier performance accurately, F/A ring oscillator was fabricated on the same wafer as the multiplier.

Functional tests were performed by randomly selected input patterns. Maximum multiplying time, τ_{mul}, is observed when the signal propagates through the bold line arrow path, as indicated in Fig.1. τ_{mul} and average power, P_{av}, vs. supply voltage, V_{DD}, relationships were obtained, as shown in Fig.3. This multiplying time depends on F/A propagation delay, τ_{FA}. Comparison between measured (F/A ring oscillator) and calculated (circuit simulation) τ_{FAs} are shown in Fig.4. They are almost the same in wide V_{DD} range. Using the simulated τ_{FA}, τ_{mul} can be estimated as $\tau_{mul} = \tau_{FA} \times 31 + \tau_{NOR} + \tau_{I/O}$. Here, τ_{NOR} and $\tau_{I/O}$ correspond to NOR gate and I/O buffer delays, respectivly. Predicted τ_{mul} shows good agreement with the experimental data, as shown in Fig.5. Performance comparison with other multipliers is shown in Fig.6. SOS CMOS has an advantage over other devices.

In conclusion, the SOS CMOS 16 bit parallel multiplier operates with τ_{mul} = 65nsec and P_{av} =250mW at V_{DD}=5V. SOS CMOS can realize expected high performance LSIs with good designability and high producibility.

References

1) N. Nikaido et. al. "An n-MOS 16 bit parallel multiplier" IECE Paper Tech. Group on Semiconductor and Semiconductor Devices SSD79-24 1979
2) F.S. Lee et. al. "High speed LSI GaAs integrated circuits" Proc. ICCC pp697-700 1980
3) Y. Ohno et. al. "Influence of Si-sapphire interface states on electrical characteristics of SOS MOSFETs", paper in preparation.
4) M. Fukuma et. al. "SOS MOSFET two-dimensional analysis", paper in preparation.

L_{eff}	1 μm
W_{eff}	8 μm
T_{ox}	230Å
T_{epi}	0.4 μm
Gate poly-Si	n^+(NMOS), p^+(PMOS)
W_{AL}	5 μm
$W_{contact}$	3 μm

Table 1 Device parameters, and design rule outline.

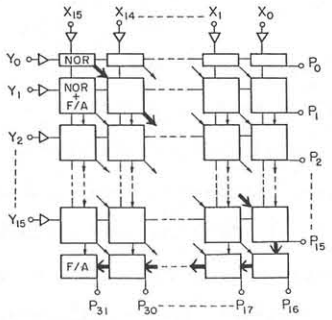

Fig.1 16 bit parallel multiplier configuration. Bold line arrow indicates critical path.

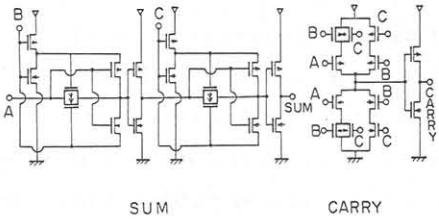

Fig.2 "Sum" and "carry" circuits.

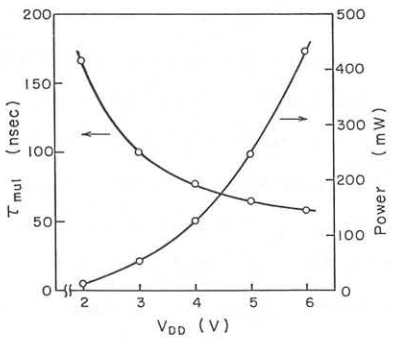

Fig.3 τ_{mul} and P_{av} obtained as a function of V_{DD}.

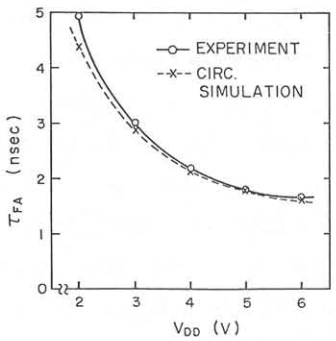

Fig.4 τ_{FA} comparison between experimental (F/A ring oscillator) and circuit simulation results.

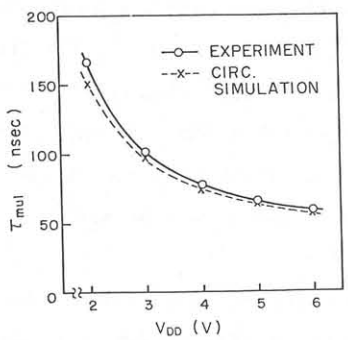

Fig.5 τ_{mul} comparison between experimental and circuit simulation results.

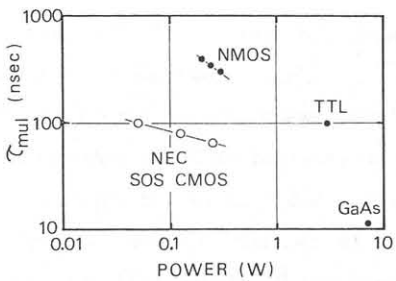

Fig.6 16 bit multiplier performances. GaAs: extrapolated from 8 bit multiplier.