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SOS CMOS 16 bit Parallel Multiplier

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As multiplication is essential in digital signal processing, many reports have
been published on multiplier LSIs1,2). In this paper, a high performance 16 bit
parallel multiplier is presented. It features SOS CMOS, which is suitable for logic
LSI applications.

The multiplier configuration is shown in Fig.1, i.e., Full adder (F/A)+NOR
cellular array. Device parameters and design rule outline are listed in Table 1.
Although Si islands were formed by conventional anisotropic-etching method, gate-
oxide break-down voltage is kept sufficiently high. Specially developed 1-D pro-
cess-device3) and 2-D device4) simulators were utilized for fine pattern SOS MOSFET
design, i.e., short-channel effect and back-channel leakage current suppressions.

In circuit and mask pattern design, special design methods, due to SOS CMOS, can be
used. "Sum" and "carry" circuits were designed separately, because of a high speed
operation requirement (Fig.2). However, occupied area increase is relatively small.
The n⁺ or p⁺ doped epitaxial Si layer is widely used as a signal line. This
leads to higher packing density and less pattern design time without any additional
parasitic capacitance. Parasitic capacitance, except at a line cross over point,
can be ignored in circuit optimization process. F/A+NOR cell size is 230x190μm
and chip size is 5.02x4.87mm. In order to evaluate multiplier performance accurately,
F/A ring oscillator was fabricated on the same wafer as the multiplier.

Functional tests were performed by randomly selected input patterns. Maximum
multiplying time, Tmul, is observed when the signal propagates through the bold
line arrow path, as indicated in Fig.1. Tmul and average power, Pav, vs. supply
voltage, VDD, relationships were obtained, as shown in Fig.3. This multiplying
time depends on F/A propagation delay, TFA . Comparison between measured (F/A ring
oscillator) and calculated (circuit simulation) TFA are shown in Fig.4. They are
almost the same in wide VDD range. Using the simulated TFA , Tmul can be estimated
as Tmul = TFA x31+TNor+TV0 . Here, TNor and TV0 correspond to NOR gate and I/O buffer
delays, respectively. Predicted Tmul shows good agreement with the experimental
data, as shown in Fig.5. Performance comparison with other multipliers is shown in
Fig.6. SOS CMOS has an advantage over other devices.

In conclusion, the SOS CMOS 16 bit parallel multiplier operates with
Tmul = 65nsec and PAV =250nW at VDD=5V. SOS CMOS can realize expected high performance LSIs
with good designability and high producibility.
References

2) F.S. Lee et. al. "High speed LSI GaAs integrated circuits" Proc. ICCC pp697-700 1980

Table 1 Device parameters, and design rule outline.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
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<tr>
<td>$L_{eff}$</td>
<td>1 $\mu$m</td>
</tr>
<tr>
<td>$W_{eff}$</td>
<td>8 $\mu$m</td>
</tr>
<tr>
<td>$t_{ox}$</td>
<td>230 $\AA$</td>
</tr>
<tr>
<td>$t_{epi}$</td>
<td>0.4 $\mu$m</td>
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<td>Gate poly-Si</td>
<td>n&quot;(NMOS), p&quot;(PMOS)</td>
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<td>W_AL</td>
<td>5 $\mu$m</td>
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<tr>
<td>W_contact</td>
<td>3 $\mu$m</td>
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Fig.1 16 bit parallel multiplier configuration. Bold line arrow indicates critical path.

Fig.2 "Sum" and "carry" circuits.

Fig.3 $T_{mul}$ and $P_{av}$ obtained as a function of $V_{dd}$.

Fig.4 $T_{FA}$ comparison between experimental (F/A ring oscillator) and circuit simulation results.

Fig.5 $T_{mul}$ comparison between experimental and circuit simulation results.

Fig.6 16 bit multiplier performances. GaAs: extrapolated from 8 bit multiplier.