A－2－3 A Low Power 8 Bit Parallel A/D Converter with High Accuracy Process

T. Takemoto, M. Inoue, H. Sadamatsu, A. Matsuzawa, Y. Hirofuji and T. Komeda
Semiconductor Research Laboratory, Matsushita Electric Industrial Co., Ltd.
3-15 Yagumo-Nakamachi, Moriguchi-Shi, Osaka 570, Japan

An increased tendency to use A/D converters for video signal processing strongly demands a high-speed, low power and high accuracy A/D converter. In a parallel A/D conversion, each comparator must make its decision at the same point in time relative to input waveform. The comparator relies on component matching to minimize comparator-to-comparator-timing skew (a factor of the apperture uncertainty) and offset voltage mismatch. The offset voltage mismatch of pair transistors, ΔV_{BE} is expressed as:

$$\Delta V_{BE} = \frac{kT}{q} \ell n \frac{\rho_{SE2} \cdot h_{FE2} \cdot S_2}{\rho_{SE1} \cdot h_{FE1} \cdot S_1} + (R_{C1} - R_{C2}) I_E$$

where ρ_{SE}, S and R_C are sheet resistivity, diffusion area and contact resistance between metal and silicon in the emitter region, respectively. Suffixes 1 and 2 indicate either of pair transistors. In our experiment, $R_{C1} - R_{C2}$ was controlled to be less than 2Ω even in 3 μm square contact area. Further distributions of emitter sheet resistance and emitter area were suppressed down to 1 - 2% by adopting ion implantation technique for emitter and 10 to 1 reduction optics wafer stepper. As a result, ΔV_{BE} value is affected mainly by h_{FE} difference. Figure 1 shows the relation of the ΔV_{BE} values between measured and calculated from measured h_{FE} difference. To improve h_{FE} difference of pair transistors, serial implantation of B^+ and As^+ was tried through the same window. Generally the ion implant causes residual defects in the base region even if it is followed by thermal annealing[1]. The leakage current of emitter-base junction across these defects region causes a variation of h_{FE}. Defect region remained only in the emitter surface region by serial implantation of B^+ and As^+ through the same window. Therefore transistor having small h_{FE} value due to large leakage current appeared only a little. Figure 2 shows the distribution of the h_{FE} for various emitter and base processes. To improve the accuracy of DC reference voltage determined by a single metal line, the mask of photolithography is produced by using electron beam. Figure 3 represents linearity error, or fraction of DC reference voltage versus output code number. As shown in Fig. 3, fractions of DC reference voltage for each comparator are less than 1/4 LSB. Low pressure epitaxial method with slight auto doping is used to reduce bipolar device size. Standard size of collector and contact are 35×22 μm^2 and 3×3 μm^2, respectively. The value of f_T of this transistor is 2 GHz. In designing parallel A/D con-

verter, optimized comparator stage was developed which was reduced both in the number of transistors and in power consumption. High speed operation was made possible by using high gain current-driven latch based on positive feedback. For the reduction of the transistors counts (17 transistors per stage), wired-or logic was introduced into the comparator. Table 1 summarizes the electrical characteristics of the 8 bit A/D converter. Since the power consumption is 800 mW, conventional package can be used which dispenses with radiation plate or fin. The figure of merit of this device[2] is 1.2×10^{10} (Hz/W), or 3 - 4 times better than that achieved by conventional 8 bit parallel converters. Figure 4 shows the reconstruction of a 10 kHz sinewave, sampled at 40 MHz to 8 bit accuracy.

This work was supported by the Ministry of International Trade and Industry of Japan.

References

1) T.E. Seidel et al., IEEE Trans. Electron Devices, ED-24, p.717 (1977)
2) G. Emmert et al., IEEE J. Solid-State Circuits, SC-15, p.1030 (1980)

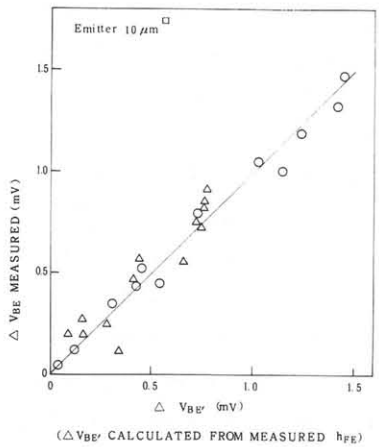

Fig.1. The relation of the V_{BE} values between measured and calculated from measured h_{FE} difference.

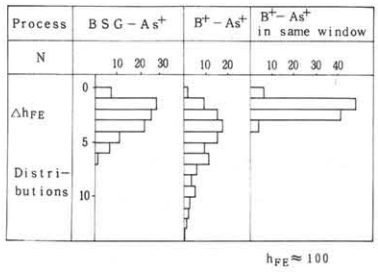

Fig.2. Typical distribution of the h_{FE} for various processes.

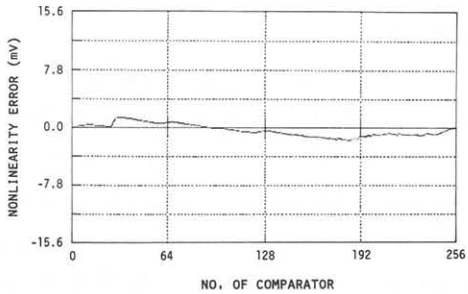

Fig.3. Fractions DC reference voltage for each comparator.

TYPICAL DATA	
RESOLUTION	8 BIT + OVERFLOW
MAXIMUM CONVERSION FREQUENCY	40 MHz
POWER CONSUMPTION	800 mW
DYNAMIC RANGE	2.0 V
LINEARITY	±1/2 LSB
APERTURE JITTER	PS
DIFFERENTIAL GAIN	1 %
DIFFERENTIAL PHASE	< 1 DEGREE
COMPONENT COUNT	7500
CHIP AREA	26.86 mm²

Table 1. Summary of significant A/D characteristics.

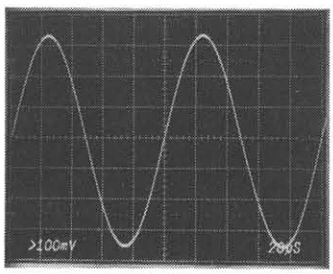

Fig.4. Reconstruction of a 10 kHz sinewave sampled at 40 MHz to 8 bit accuracy.