

A-2-4 Threshold Difference Compensating Sense Amplifier for High Density Dynamic MOS RAM's

T.Furuyama, S.Saito and S.Fujii

Semiconductor Device Engineering Laboratory

Toshiba Corporation, Kawasaki, Japan

A dynamic flip-flop sense amplifier, which basically consists of two driver MOS transistors, is widely used in VLSI memories. However, a threshold difference ΔV_T between the two transistors has become one of the severest problems especially in high density dynamic MOS RAM's. Several sense amplifiers have been presented to obtain a large S/N ratio [1]-[2], or to compensate the threshold difference [3]-[4].

In this paper, a new threshold difference compensating sense amplifier technique for high density dynamic RAM's is described.

A typical 256K dynamic RAM will have 1024 sense amplifiers. The distance between two driver transistors of the sense amplifier is as long as 50 μ m. Typical ΔV_T distributions of paired transistors, which are about 50 μ m away from each other, are shown in Fig.1, for two different effective channel lengths. The distribution of 1.5 μ m transistors is broader than that of 2.0 μ m transistors because of size effects. The standard deviations σ are 12.6mV and 11.1mV for 1.5 μ m and 2.0 μ m transistors, respectively. Considering the number of sense amplifiers, the ΔV_T contribution to the sensitivity of conventional sense amplifiers can be roughly estimated as $3\sigma/(S/N \text{ ratio})$. So the sensitivity might easily exceed 500mV in the case of high density memories beyond 256K dynamic RAM.

To acquire higher sensitivity, a new ΔV_T compensating sense amplifier is introduced. An equivalent circuit and a timing diagram are shown in Fig.2 and Fig.3. Initially, paired bit lines of different levels are connected each other. Then, sense node N_1 and N_2 are precharged to V_{CC} level through T_3 and T_4 , maintaining N_1 and N_2 to have the same potential. As a result, bit lines BL_1 and BL_2 are precharged to $V_{CC}-V_{T1}$ and $V_{CC}-V_{T2}$ through sense amplifier driver transistors T_1 and T_2 , respectively, where V_{T1} and V_{T2} are the threshold voltages of T_1 and T_2 . Subsequently T_5 and T_6 are turned on to connect each bit line and sense node, so a cross-coupled flip-flop organization is composed. The bit line potentials V_{N1} , V_{N2} are presented as follows, where C_B and C_N are the bit line and the sense node capacitance,

$$V_{Ni} = V_{CC} - \frac{C_B}{C_B + C_N} \cdot V_{Ti} \quad (i=1,2).$$

Then, a certain word line is selected, and sensing operation starts as conventional amplifiers. The ΔV_T contribution to the sensitivity is described as follows, for a new sense amplifier and a conventional one, where C_S is a storage capacitance,

$$V_{\Delta V_T\text{-compensating}} = \left(\frac{C_N}{C_S} + 1 \right) \cdot \Delta V_T$$

$$V_{\text{conventional}} = \left(\frac{C_B + C_N}{C_S} + 1 \right) \cdot \Delta V_T.$$

Assuming that C_S , C_N and C_B are 40, 50 and 250fF respectively, $V_{\Delta V_T\text{-compensating}}$ and $V_{\text{conventional}}$ are calculated as $2.25 \cdot \Delta V_T$ and $8.5 \cdot \Delta V_T$.

To evaluate a new sense amplifier, a test device, shown in Fig.4, is designed and fabricated. This new amplifier can also operate as a conventional amplifier, when ϕ_T is always fixed to V_P level. This enables an accurate comparison between both types of amplifiers, using the same test sense amplifier. Fig.5 shows the measured and calculated data. Here, sensitivity is defined as a minimum cell signal, which can be sensed correctly. A good agreement between the measurement and the calculation is obtained, and the sensitivity of a new amplifier is four times higher than that of a conventional one.

In conclusion, the new ΔV_T compensating sense amplifier technique is introduced. Both of theoretical and experimental data show remarkable sensitivity improvement. This technique will become important for high density memories beyond a 256K dynamic RAM.

The authors wish to thank H.Hara and Y.Nishi for the encouragement, Y.Uchida, K.Ohuchi, O.Ozawa and T.Mochizuki for their helpful discussions and sample fabrications.

References

- [1] L.G.Heller, D.P.Spampinato and Y.L.Yao, IEEE J. Solid-State Circuits, vol.SC-9, pp.596, Oct.1976.
- [2] L.G.Heller, ISSCC 79, Digest of Technical Papers, pp.20, Feb.1979.
- [3] S.Suzuki and M.Hirata, IEEE J. Solid-State Circuits, vol.SC-14, pp.1066, Dec.1979.
- [4] T.Iizuka, T.Ohtani, T.Sato and H.Tango, Japanese J. Appl. Phys., vol.18 Suppl.18-1, pp.51, 1979.

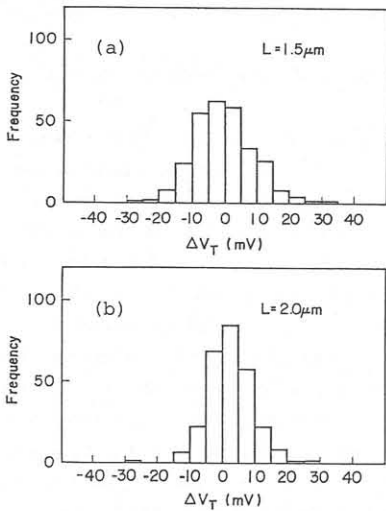


Fig.1 Typical ΔV_T distributions of two effective channel length transistors. Gate oxide thickness is about 300Å.

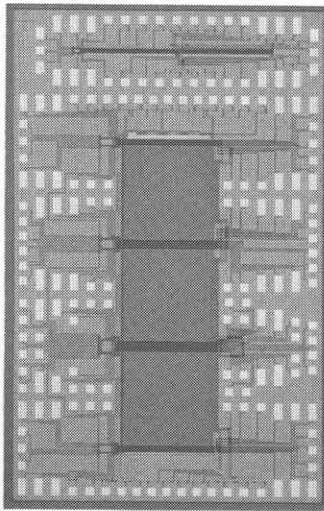


Fig.4 A microphotograph of the test device chip.

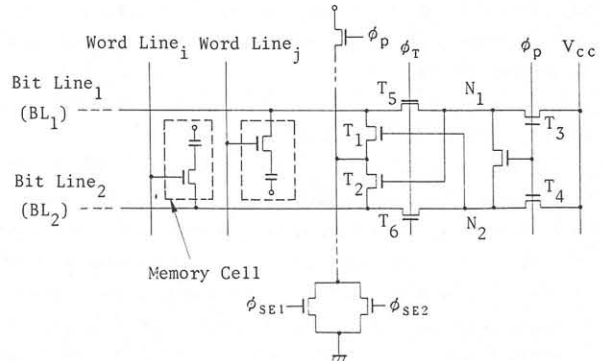


Fig.2 An equivalent circuit of the new ΔV_T compensating sense amplifier.

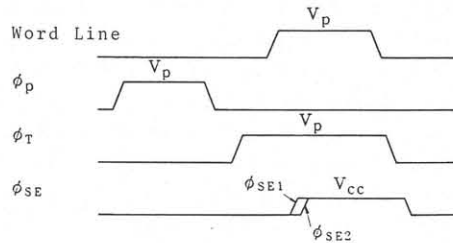


Fig.3 A timing diagram of the new sense amplifier. V_P satisfies $V_P > V_{CC} + V_T$.

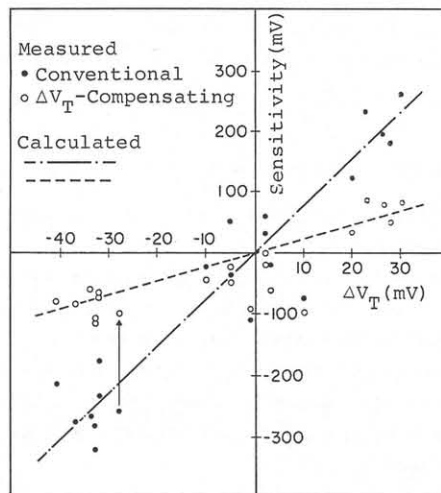


Fig.5 Measured and calculated sensitivity of the new sense amplifier and a conventional one.