A — 2 — 6   Soft Error Rate Analysis Model(SERAM) for Dynamic NMOS RAMs

Masaaki Aoki, Toru Toyabe, Takashi Shinoda[*], Toshiaki Masuhara,

Shojiro Asai, Hiroshi Kawamoto[*] and Kazumichi Mitsusada[*]

[*]Central Research Laboratory, Hitachi Ltd., Kokubunji, Tokyo, Japan
Device Development Center, Hitachi Ltd., Kokubunji, Tokyo, Japan

As the trend in dynamic RAMs is toward higher levels of integration, evaluating alpha-particle induced soft error[1] rates prior to device design has become increasingly more important. Although several works[2,3] have been reported for modelling collection processes, computation of error rates for the RAM arrays has not been satisfactory. This paper presents a new model, called Soft Error Rate Analysis Model(SERAM), to precisely predict error rates of dynamic NMOS RAMs. SERAM simulates the three-dimensional diffusion and collection processes of generated carriers for various alpha-particle incidences. The noise charge induced by alpha-particle was measured to verify SERAM.

SERAM is as follows: The electrons generated within the depletion region beneath the collector are instantaneously collected. A part of electrons generated in the field-free substrate region diffuse and are collected in the depletion region. The total collected charge, Q_α, is a sum of both charges computed by considering the ionization density for alpha-particle in Si. The frequency (the probability distribution, $D(Q)$) of collected charge is obtained by simulating many incidences with various energies, locations and angles of incidence, and by sorting the collected charges. The upset probability of stored data for one incidence is given by the equation: $\varepsilon = \int_{Q_c}^{\infty} D(Q)dQ$, where Q_c is the critical charge for upset. An alpha-particle causes noise charge in a cell or a bit line. The soft error rate for memory cell mode is given by $E_r^{(M)} = \Phi_\alpha N a \varepsilon$, where Φ_α is the alpha flux; N is the number of cells; and a is the alpha radiated area per one collector. The soft error rate for bit line mode is given by $E_r^{(B)} = \frac{t_f}{t_{RC}} \Phi_\alpha \frac{N_b}{2} \sum_i a_i \varepsilon_i$, where t_{RC} is the cycle time; t_f is the floating time; and N_b is the number of bit lines. The summation is done over all diffusion regions connected with one bit line.

To verify the model, we measured the noise charge collected in one memory cell of a sample. The sample was fabricated by the conventional double polysilicon gate process. The area of the storage gate was $18 \times 18~\mu m^2$. The transient voltage pulses generated when a charge collected within the cell were sensed by a source follower circuit, as shown in Fig.1. The waveforms of the output pulses were measured using the biomation 8100 waveform recorder. The tipical waveforms are shown in Fig.2. The collection time estimated from the falling time was about 20 to 100 nanoseconds. The total collected charge was determined by the peak value. The measured and computed frequencies are shown in Fig.3. The agreement between the simulation and the experiment is good.

We have measured and analyzed the error rates for 64K-bit samples. The critical charge dependence of the error rate was shown in Fig.4. The bit line mode error was dominant for the samples with the critical charge of cell above 80 fC. Agreement with the experiment was excellent for this mode.

In addition, memory cell scaling analysis shows that if the cell area scales as $(1/K)^2$, the ratio Q_c/Q_α decreases as $(1/K)^\beta$, where $K>1$, $\beta \sim 0.4$ for unscaled voltages and 1.4 for scaled voltages.

In conclusion, we have developed SERAM which analyzes the alpha-particle induced soft error rates of dynamic NMOS RAMs. Our model will provide an effective design tool for evaluating the alpha-immunity of dynamic RAMs with the capacity of 256K-bit, 1M-bit or larger.

References: 1) T.C.May and M.H.Woods, IEEE Trans. on Electron Devices,ED-26,2(1979) 2) S.Kirkpatrick, IEEE Trans. on Electron devices,ED-26,1742(1979) 3) G.A.Sai-Halasz and M.R.Wordeman, IEEE Electron Device Letters, EDL-1,211(1980)

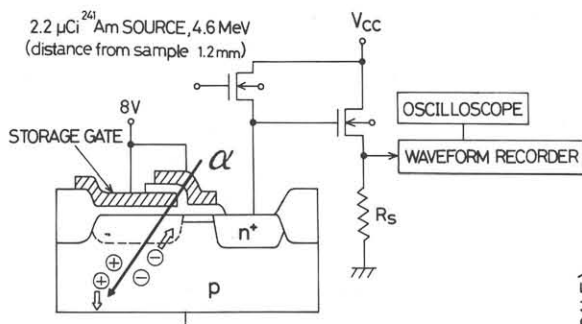Fig.3 Measured and computed frequencies for one memory cell

Fig.1 Dynamic NMOS memory cell cross section and the experimental setup for measuring the noise charge
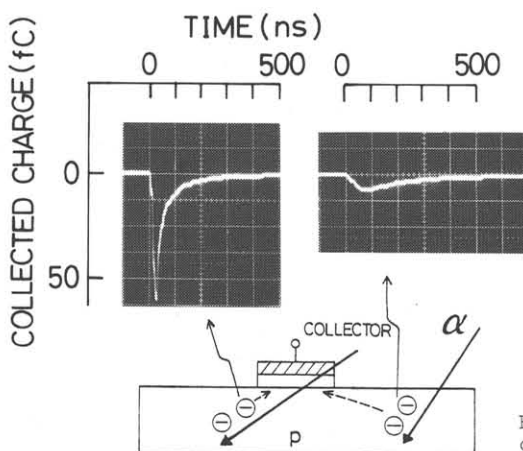
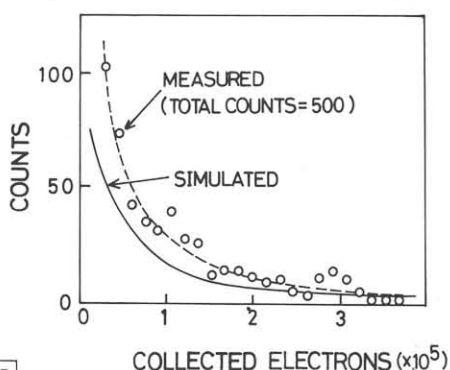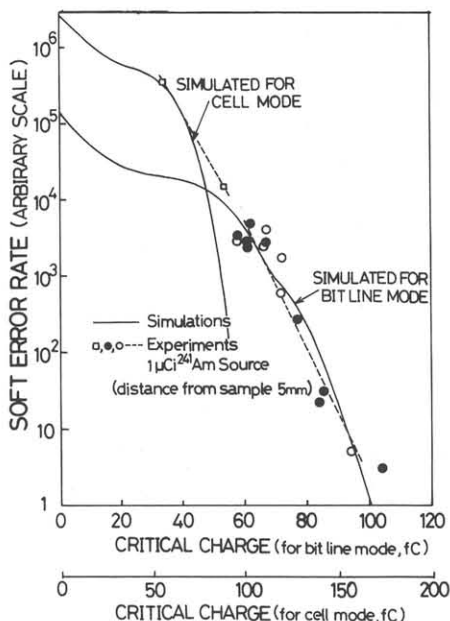
Fig.2 Typical transient waveforms of collected charges

Fig.4 Soft error rate versus critical charge for samples of 64K dynamic NMOS RAMs. Number of incidences calculated to construct one curve was approximately 10^6.