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A-2-7 Novel High Alpha-Particle-Immunity and High Density d-RAM Cell

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A new dynamic RAM cell with dynamically switched buried channel (DSC cell), and with readout signal gain is proposed. The cell has extremely small collection efficiency of charges generated by alpha-particle, and allows large amount of leakage charges due to its peculiar structure, therefore can achieve high packing density, compared with any other proposed cells such as SCM[1], TI RAM cell[2] and DMOS cell[3].

Fig. 1 shows DSC cell structure and its equivalent circuit. DSC cell is composed of an MOSFET, an MOS capacitor and a JFET with a buried channel under the MOS capacitor. The buried channel is cut off when charges are stored in the capacitor through the MOSFET ("1" state), then readout current does not flow between WB and RW lines. While it is not cut off when no charges are stored ("0" state), then the current flows.

Experimental test devices were fabricated using double polysilicon and FIPOS[4] techniques. Fig. 2 shows write and readout waveforms. Since readout current of DSC cell is due to electrons injected from N^+ layer to the P region, large readout current can be obtained, compared with unipolar JFET, as shown in Fig. 3.

Permitted numbers of leakage charge N_e in DSC cell is large compared with other gain cells, because large surface-potential can be applied under the capacitor without charge injection from substrate (i.e., the insulator or reverse-biased N layer). It was experimentally confirmed that N_e in DSC cell is described by

$$N_e = S_c \cdot (C_{ox} \cdot (V_{si} - V_{sf})/q + \Delta W \cdot N_A), \quad (1)$$

$$V_{sf} = qN_A d^2/(2K_{Si}\varepsilon_0) - 2\varphi_F, \quad (2)$$

$$\Delta W = \sqrt{2K_{Si}\varepsilon_0/(qN_A)}(\sqrt{2\varphi_F + V_{si}} - \sqrt{2\varphi_F + V_{sf}}), \quad (3)$$

where S_c is capacitor area, C_{ox} is gate oxide capacitance, V_{si} is surface potential of writing level, V_{sf} is surface potential at which dynamic deep depletion layer width becomes equal to the P region thickness d, and ΔW is change of the depletion layer width due to ΔV (= $V_{si} - V_{sf}$). N_A dependences of N_e/S_c and ΔV are shown in Fig. 4. From Fig. 4, it is found that DSC cell has large N_e, which is based upon large ΔV.

The collected numbers of alpha-particle-generated electrons N_α in DSC cell is very much small, because the P region is sufficiently thin and diffusion component of electrons generated beneath the depletion layer is negligible due to insulator substrate or built-in mechamism. Fig. 5 shows calculated minimum capacitor area required to hold stored "1" state for 4 msec, for typical leakage current flow of 1 $\mu A/cm^2$[5] at 90°C and one strike of typical 5 MeV alpha-particle with incident angle of 45°. From Fig. 5, it is found that capacitor area of DSC cell can be extremely reduced, which is based upon both small N_α and sufficient N_e.

Comparison among DSC cell, other gain cells and single transistor cell is summerized in Table 1. DSC cell is the most competent device for high packing density and alpha-particle-immunity in the future.

References
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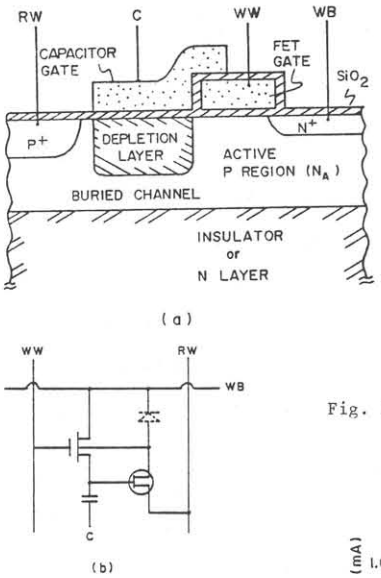

Fig. 1. (a) DSC cell structure, (b) Equivalent circuit of DSC cell.

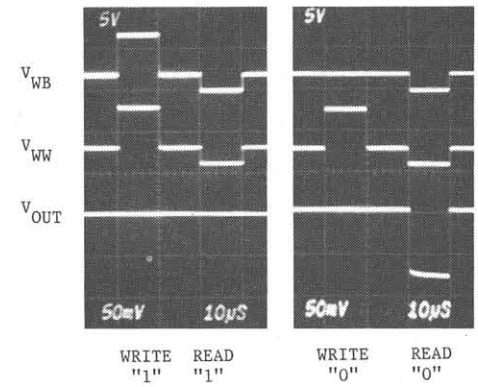

Fig. 2 Write and readout waveforms. (a) "1". (b) "0". (V_c=5 V. 100Ω resistor is connected between RW line and ground.)

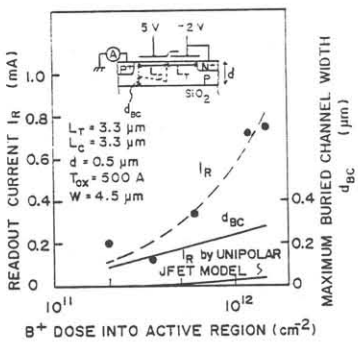

Fig. 3 N_A dependence of Readout current.

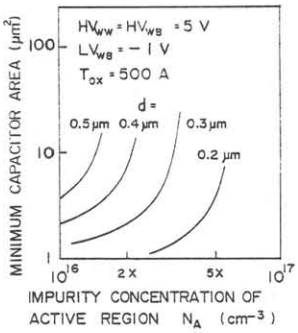

Fig.5 N_A dependence of calculated minimum capacitor area.

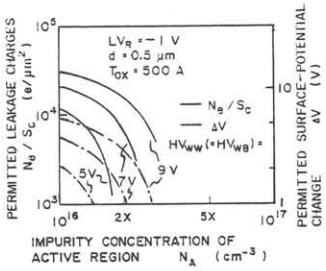

Fig. 4 N_A dependences of leakage charge per unit area and permitted surface potential change.

Table 1. Comparison of d-RAM cells.

	DSC		TI	SCM	DMOS	1 Tr
Design Rule (μm)	1	3	3	3	3	2
Cell Size (μm^2)	18	79	75	90	131	70
Capacitor Area (μm^2)	3	9	9	9	49	20
Permitted Leakage Charges (C)	3.3×10^{-15}	1.2×10^{-14}	$\sim4\times10^{-15}$	$\sim8\times10^{-15}$	1.8×10^{-14}	4.1×10^{-14}
Collected Number of Alpha-Particle-generated electrons (C)	3.2×10^{-15}	3.8×10^{-15}	$\sim1\times10^{-14}$	$\sim1\times10^{-14}$	6×10^{-14}	2.2×10^{-14}
Alpha-Particle Numbers Inducing Soft Error	1	3	~ 0.4	~0.8	0.3	1.9