A－3－3 Deep Levels Induced in Annealed CZ Silicon

Kousuke IKEDA and Hidetoshi TAKAOKA

Musashino Electrical Communication Laboratory, NTT

Musashino-chi, Tokyo, 180 Japan

Deep levels are considered to reveal the electrical properties of defects. However, the electrical nature of defects which are induced by the thermal process is rarely understood. This paper reports the results of investigation on defects and their electrical properties induced in annealed CZ silicon, using transmission electron microscopy (TEM) and deep level transient spectroscopy (DLTS).

The samples used in this work were boron doped p-type (100) silicon wafers grown by the Czochralski technique, having a $3\times10^{15}cm^{-3}$ carrier concentration. These wafers contain about $10^{18}cm^{-3}$ interstitial oxygen. In order to study the electrical natures of oxide precipitate (OP), dislocation loop (DL) and stacking fault (SF), each defect was produced by individually selected annealing conditions. Table I shows the annealing conditions.

The defects in surface and bulk layers were observed by Wright solution etching method and TEM. Here, the defect distributions are regarded as uniform at the bulk layer, where an about 50μm surface layer was etched off. The defect observation results are shown in Table I. At the bulk layer, OPs, DLs and SFs were induced separately, corresponding with the annealing temperature in specimens D7, D8 and D11, respectively. On the other hand, both DLs and SFs were observed in C10. Oxide precipitates which are the origin of DLs or SFs, however, were contained in all specimens.

Schottky diodes were prepared by evaporating aluminum onto the surface layer or about 50μm etched layer. DLTS measurements were carried out for these Schottky diodes. Figure 1 shows its typical spectra. The activation energies capture cross-sections and densities for deep levels, are summarized in Table II. In the as-grown crystal (D0), DLTS peak wasn't detected and was less than the sensitivity, $\Delta C/C \simeq 5\times10^{-4}$. On the surface, the majority carrier trap $E_v+0.46eV$ (H1) was detected in the D6 specimen. In the C10, two defect energy levels, located at $E_v+0.46eV$ (H2) and $E_v+0.40eV$ (H3), were found. Both H1 and H2 are the same traps, since the activation energy and capture cross-section for both traps are almost equal. It is considered that these traps, H1 and H3, coincide with $E_v+0.48$ and $E_v+0.45eV$[1] reported by Gerson et al. It seems that fast cooling is the main cause for these traps.

In the bulk layer, only one majority carrier trap was observed for the specified sample. The energy levels, located at $E_v+0.47$, $E_v+0.55$ and $E_v+0.63eV$, were measured in specimens which contained OPs,DLs and SFs, respectively. The higher the annealing temperature is, the higher the trap activation energy is. Lefevre[2]

reported that a trap level at E_c-0.49eV in n-type FZ silicon is caused by interstitial silicon atoms, which form the DL. The DLs observed in this experiment also were of interstitial type. The difference between E_v+0.55 and E_c-0.49 eV seems to reflect the contained oxygen density. That is, the DL energy level becomes deep with the decoration of oxygen.

There is a very large difference between trap density and defect density. To explain this difference, two assumptions were prepared. The first assumption is that a defect strain is the main origin of the defect levels. The energy values in this investigation correspond to the degree of each defect strain. The Second is that the strain is strongest around the defect edge and is negligible at other parts. Under the above assumptions, it is considered that the trap density must be compared with an effective defect density, which means the product of the defect density and the number of defect edge atoms. Table III shows the effective density computed by the diameter of each defect and so on. As is evident from Table III , strong correlation is observed between trap density and effective density.

In summary, deep levels induced in annealed CZ silicon corresponding with annealing conditions, were measured by using DLTS and TEM. The trap density nearly agreed with the defect density, considering the defect strain effect.

The authors would like to thank Mr. Y. Yoriume, Dr. N. Inoue and Mr. M. Yamaguchi for their helpful advice.

References 1) J. D. Gerson et al.:J. Appl. Phys. 48 (1977) 4821.
2) H. Lefevre: Appl.Phys. 22 (1980) 15.

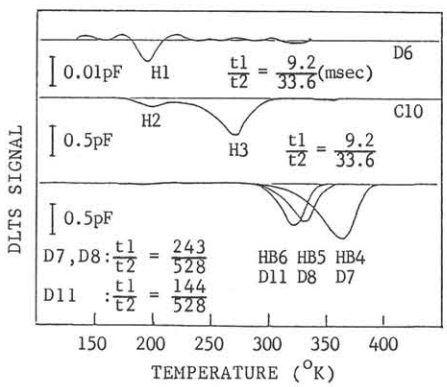

Fig. 1 DLTS spectra for B-doped CZ silicon after various annealings.

Table I Annealing conditions and defects.

	Annealing Condition (N_2 gas)	Defect	
		Surface	Bulk
D 0	As-grown	# NO	NO
D 6	650°C 3h	# NO	NO
C10	650°C 3h+1000°C 10h	# NO	DL+SF
D 7	750°C	NO	# OP(~10^{11}cm^{-3})
D 8	750°C 100h+ 870°C 75h	NO	# DL(~10^{10}cm^{-3})
D11	750°C 100h+1100°C 1h	YES	# SF(3×10^{9}cm^{-3})

* DLTS measurements were carried out at # samples.

Table III Effective density for each defect

Defect		OP	DL	SF
Diameter	(μm)	0.1	1	3
Thickness	(nm)	2	4 a	3 a
Defect density	(cm^{-3})	~10^{11}	~10^{10}	~3×10^{9}
Effective density	(cm^{-3})	~1×10^{15}	~4×10^{14}	~3×10^{14}
Trap density	(cm^{-3})	~9×10^{14}	~1×10^{15}	~9×10^{14}

* "a" is the silicon bond length(0.23nm).

Table II Hole trap characteristics in CZ-Si

	Trap	ΔE(eV)	σ(cm^2)	N_t(cm^{-3})
D 0				
D 6	H 1	0.46	8×10^{-13}	~ 1×10^{13}
C10	H 2	0.46	5×10^{-13}	~ 8×10^{13}
	H 3	0.40	9×10^{-18}	~ 6×10^{14}
D 7	HB4	0.47	3×10^{-20}	~9×10^{14}
D 8	HB5	0.55	3×10^{-18}	~1×10^{15}
D11	HB6	0.63	1×10^{-16}	~9×10^{14}

* H: Surface trap, HB: Bulk trap