A－3－7 A Novel Technology for Self-Aligned Contact Formation

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A new processing technology that is effective to prepare self-aligned contact holes is demonstrated. This technology utilizes silicon nitride films as oxidation masks to conduct selective oxidation of polysilicon gates. With this technology, MOSFETs with self-aligned contact holes have been successfully fabricated without off-set problem in transistors.

In recent several years, various technologies for self-aligned contact formation have been proposed.[1.2.3.4] In these technologies, formation of thick insulating film on polysilicon gate is required to reduce the stray capacitance between multilayered interconnections.

This problem has been overcome by utilizing oxidation-barrier effect of thermally grown nitride film[5.6.7] in our technology. Fig.1 shows key processing steps of the self-aligned contact formation technology. After the definition of polysilicon gate, As^+ ion is implanted with around $10^{14}/cm^2$ doses and with 100 to 150 Kev energy. With oxidation of the wafer and with the subsequent slight etching, oxide of 1000 to 3000 Å thickness is prepared to cover the polysilicon gate as shown in Fig.1-c. The exposed silicon surfaces are then selectively converted to uniform silicon nitride layers by heating in a purified ammonia containing gas at 1000 to 1050°C as shown in Fig.1-d. The thickness of nitride film has been found to depend on the As^+ ion doses, particularly over $10^{16}/cm^2$ as shown in Fig.2.

Subsequently, the oxide on the polysilicon gate is grown thicker through the 2nd oxidation, while oxide film is barely formed on the silicon nitride layers. As shown in Fig.3, oxidation-barrier effect has been ensured for up to 40min oxidation interval in pyrogenic H_2-O_2 gas at 900°C. This effect depends on the As^+ ion doses. The oxide thickness ratio between polysilicon gate and silicon substrate can be enhanced easily to 80 as shown in Fig.4. In the final step, the nitride films are etched away and another n^+- doped polysilicon is deposited to complete the device. This polysilicon acts as diffusion sources to form the source/drain p-n junctions.

With this technique, self-aligned contact holes have been successfully fabricated as shown in Fig.5. When the self-aligned contact holes are constructed in MOSFETs, the dielectric field strength of the oxide on polysilicon gate becomes more important. As shown in Fig.6, the breakdown voltage is high enough for interlevel insulator between multilayered interconnections.

In conclusion, MOSFET with self-aligned contact holes can be successfully fabricated, using the oxidation-barrier effect of thermal nitride films grown selectively on silicon surfaces. This technology will be useful to fabricate silicon MOS VLSIs of reduced design rules in the future.

Acknowledgement----- Authors would like to thank T. Goto, T. Okada, K. Sekito and H. Yamamoto for their encouragement and helpful discussions.

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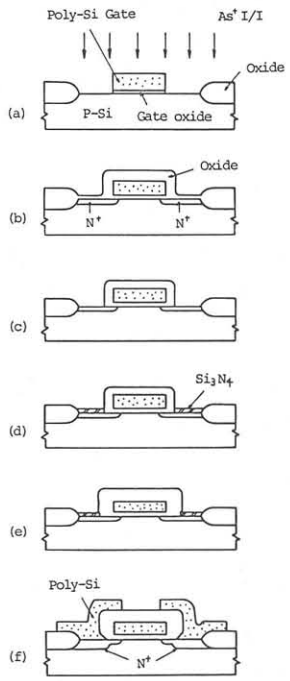

Fig.1 Schematic illustration of the self-aligned contact process.

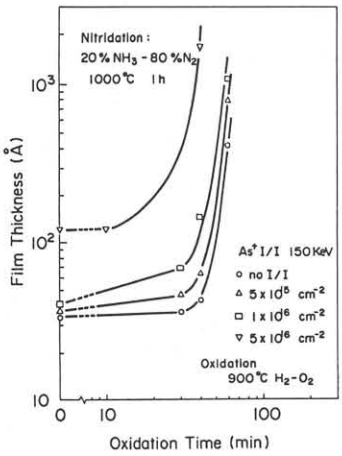

Fig.3 Oxidation-barrier effect of silicon nitride film as a parameter of As^+ ion dose

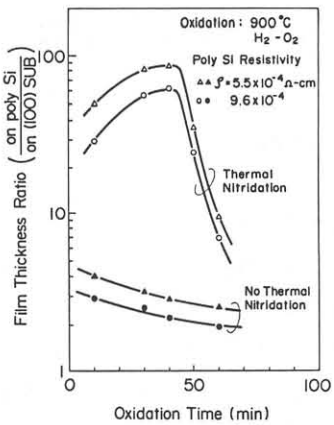

Fig.4 Film thickness ratio as a function of oxidation time.

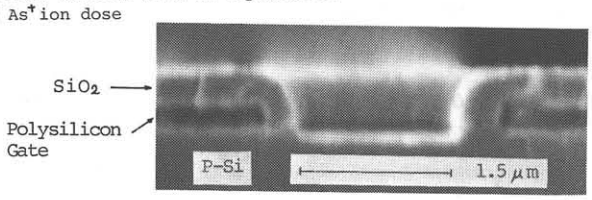

Fig.5 Cross sectional photograph of self-aligned contact.

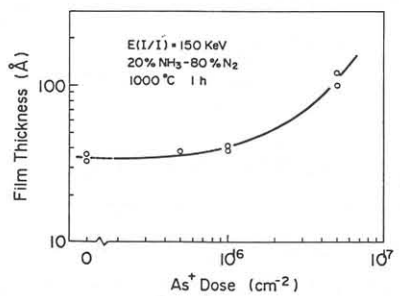

Fig.2 Dependence of the thermally grown silicon nitride film on As^+ dose.

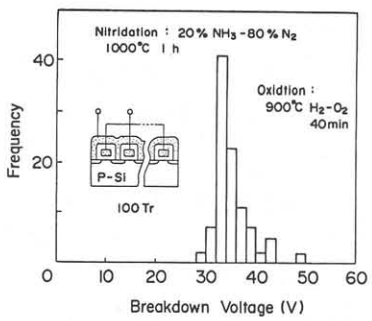

Fig.6 Breakdown voltage distribution of the oxide grown around the 100 SAC transistor polysilicon gates.