A −4 −2 Recrystallization of Silicon Film on Nitride/Oxide double Insulating Structure by CW Laser Irradiation

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Considerable interest has been recently focussed on a silicon-on-insulator (SOI) material system by using lasers in recrystallization of deposited polysilicon[1-5]. Some techniques[3-5] for device fabrication have been reported in which a thick oxide layer was used as an insulating layer. Though the polysilicon deposited on a thin silicon nitride layer is easier to recrystallize with laser irradiation than that on an oxide layer[1], the nitride is not used as an insulating material because it is difficult to get enough thickness for isolation from the substrate without any cracking.

In this paper double layer structure of thin nitride on oxide is proposed as the insulating layer, which makes polysilicon more tolerant to be stripped off at high laser power. Very large and superior recrystallized polysilicon layer can be obtained and is applied for a fabrication of a Bipolar transistor (Bip-Tr) by using this structure and optimizing laser scan step. Polysilicon layers by three kinds of deposition techniques are investigated. But clear difference in recrystallization phenomena between them can not be found.

The supporting substrates were p-type silicon wafers with (100) orientation. A 5000 Å thick layer of oxide was thermally grown on the wafers and a 750 Å thick layer of CVD nitride was subsequently deposited on some wafers to form a nitride substrate. A 1 μm thick layer of polysilicon was then deposited by using three kinds of techniques. One was the conventional LPCVD technique at 630 °C (poly-Si-A). Others were the epitaxial growth technique in which two kinds of polysilicon were deposited. They were epitaxially grown polysilicon at 930 °C at normal pressure (poly-Si-B) and polysilicon at 1080 °C at reduced pressure (poly-Si-C) by using SiH_4 and SiH_2Cl_2 as source gas, respectively. The poly-Si-C could be deposited on the nitride substrate, but not stably on oxide substrate.

The samples were then irradiated with a cw-Ar scanning laser. A sample holder temperature was kept constant at 450 °C throughout the present experiment. Laser irradiating conditions were as follows : Output power of 8 W to 12 W, Spot size of 60 μm to 80 μm, Scan step for overlapping of 5 μm to 50 μm, and Scan rate of 12.5 cm/sec.

The samples were then examined by using an optical microscope with an interference contrast attachment and Sirtl etching to decorate the grain boundaries which was found to be correlated with an internal microstructure examined by TEM analysis.

Figure 1 shows typical optical micrographs of recrystallized polysilicon on nitride and oxide substrate, respectively. Polysilicon on oxide tends to be stripped off as laser power becomes higher. This is considered to be due to large thermal expansion coefficient of oxide compared with those of nitride and silicon. So relatively low power should be used to get an uniform recrystallization in a wafer and results in long grains as shown in Fig.2-(a). But the nitride substrate makes polysilicon more tolerant to be stripped off at high power level, and results in a large grain growth with high power laser irradiation as shown in Fig.2-(b).

With decreasing the laser scanning step size less than 10 μm, the lateral grain growth was observed remarkably. Figure 3 shows the change of etched surfaces observed by optical microscopy depending on the scanning step size.

Though each laser power level between three kinds of polysilicon for recrystallization

shifted slightly, any difference in recrystallized grain size and electrical characteristics in fabricated devices stated as follows could not be found.

Using the above mentioned recrystallized polysilicon layers on nitride as starting substrate, a fully isolated Bip-Tr was fabricated with the oxide isolation technique. Figure 4 shows the schematic cross section. Base, Emitter and Collector contact were implanted with boron (50 kV , $2x10^{14}/cm^2$) and arsenic (150 kV, $4x10^{15}/cm^2$), respectively. Each ion implantation was followed by the annealing step in the N_2 ambient. The junction leakage current (I_{CBO} , at V_{CBO}= 10 V) distributed widely in a wafer, but those of devices which showed a transistor action exsisted from 1 pA to 20 pA. These values were comparable to or about one order of magnitude higher than those of conventional ones in bulk silicon. An example of the I_C-V_{CE} characteristics of the transistor in poly-Si-C is shown in Fig.5. The current gain h_{FE}, BV_{CBO}, BV_{CEO}, and BV_{EBO} were 29, 73 V, 30 V and 5.2 V, respectively.

References 1) A. Gat et al: Appl. Phys. Lett., 33(1978)775. 2) A. F. Tasch et al: Elect. Lett., 15(1979)435. 3) H. W. Lam et al: IEEE Elect. Dev. Lett., EDL-1(1980)206. 4) H. W. Lam et al : Extended Abstract, ECS Meetin, Hollywood, Florida, Oct.1980. 5) M. W. Geis et al: Appl. Phys. Lett., 35(1979)71

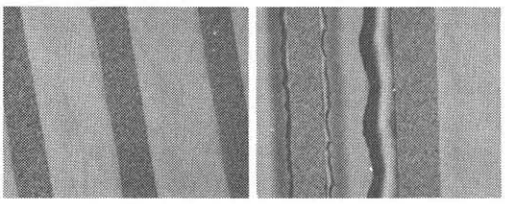


Fig.1 Optical micrographs of the recrystallized polysilicon on nitride substrate--(a) and on oxide substrate--(b)

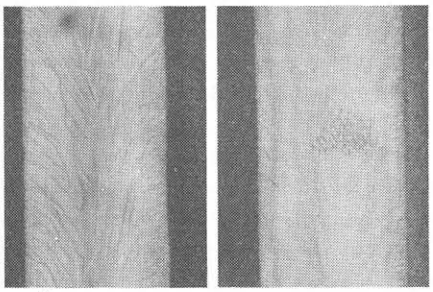
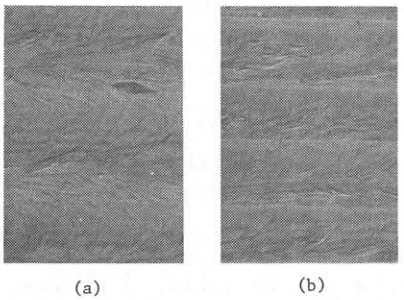


Fig.2 Optical micrographs of etched surfaces
(a) recrystallized polysilicon on oxide at 10 W.
(b) recrystallized polysilicon on nitride at 12.5 W



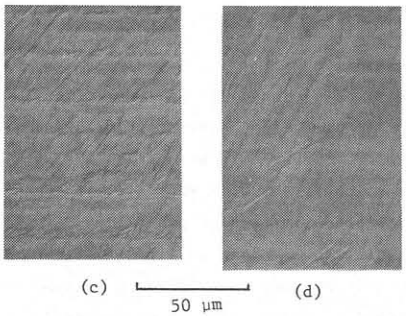


Fig.3 Surface structure depending on the scanning step size
(a) 50 μm/step at 9.7 W (b) 30 μm/step at 9.7 W
(c) 10 μm/step at 9.3 W (d) 5 μm/step at 8.7 W

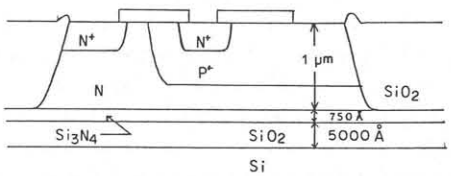


Fig.4 Cross sectional view of Bip-Tr. in SOI.

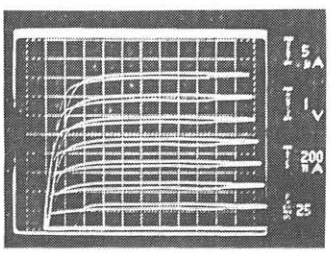


Fig.5 I-V characteristics