A −4 −3

IMPROVEMENT OF SOS DEVICE PERFORMANCE BY SOLID-PHASE EPITAXY

Toshio YOSHII, Shinji TAGUCHI*, Tomoyasu INOUE and Hiroyuki TANGO*

Toshiba R and D Center, Semiconductor Device Engineering Laboratory*, TOSHIBA CORPORATION

1 Komukai-Toshiba-cho, Saiwai-ku, Kawasaki 210, Japan

It is well known that crystalline quality of Si films on sapphire (SOS) markedy affects device characteristics, such as drain leakage currents and carrier mobilities. Recently, it has been reported that crystalline disorder near the Si-sapphire interface is reduced by solid-phase epitaxy (SPE) after amorphization, whereas crystallinity in the surface region is kept as it is deposited. [1)-3)] This paper describes significant improvement in SOS device characteristics by doubly applying SPE technique to both surface and interface regions in SOS films.

P-type Si films of 0.3 μm thick were epitaxially grown on sapphire using the pyrolysis of SiH_4. The samples were amorphized by Si ion implantation, and recrystallized by furnace annealing at 1000°C in an N_2 ambient for 20 min. Test devices were fabricated using Si-gate CMOS process. First, improvement in the interface region of SOS films was achieved by Si ion implantation with 1×10^{15} cm^{-2} at 190 keV (R_P = 2952Å) and subsequent thermal annealing. Second, Si surface region was amorphized by Si ion implantation with 2×10^{15} cm^{-2} at 100 keV (R_P = 1469Å) and recrystallized from the inner region of the film towards the surface. After the second SPE, effective mobilities of N-channel and P-channel transistors are 510 and 225 $cm^2/V.sec$ at $V_G - V_T$ of 4 V, as shown in Fig. 2, which are 1.3 times and 1.1 times larger than those of as-grown samples, respectively. A significantly reduced drain leakage current of 1.8×10^{-12} A/50 μm for N-channel transistors is obtained, whose value is about 1/100 of those in the as-grown samples, as shown in Fig. 3. The higher mobility and lower leakage current thus obtained, should be attributed to the drastic improvement of crystalline quality in the whole region of SOS films by the double SPE.

The mechanism behind the above improvement has been also investigated.

After the first SPE, drain leakage current in N-channel transistors has a minimum value of 1×10^{-11} A/50 μm at 1×10^{15} cm^{-2}, as shown in Fig. 4, which is one order of magnitude smaller than that in as-grown sample. On the contrary, as shown in Fig. 5, effective mobilities of both N-channel and P-channel transistors in the SPE samples are nearly the same as those in as-grown samples. This clearly suggests that improvement in crystalline quality is limited only in the interface region but crystalline quality in the surface region still remains unchanged.

Consequently, the improvement in both mobility and leakage current can be realized only when SPE is doubly applied to SOS structure as described in the present paper.

The present technique will offer greater feasibility for the SOS technology in the future VLSI era.

ACKNOWLEDGMENT:

The authors wish to thank Mr. Koike for the Si ion implantation.

REFERENCE:

(1) S.S. Lau, S. Matteson, J. W. Mayer, P. Revesz, J. Gyulai, J. Roth, T. W. Sigmon and T. Cass, Appl. Phys. Lett., 34, P76, 1979.

(2) T. Inoue and T. Yoshii, Appl. Phys. Lett., 36, P64, 1980.

(3) M. E. Roulet, P. Schwob, I. Golecki and M.-A. Nicolet, Electronics Lett., 15, P527, 1979.

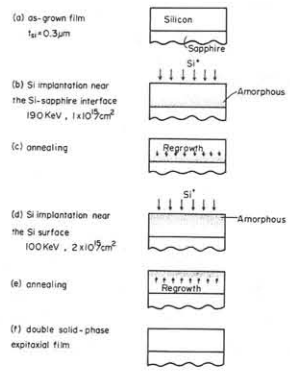

Fig. 1. Double SPE processing steps.

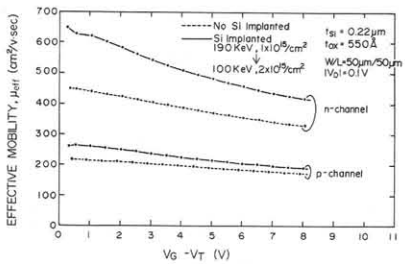

Fig. 2. Effective mobilities as a function of gate voltage.

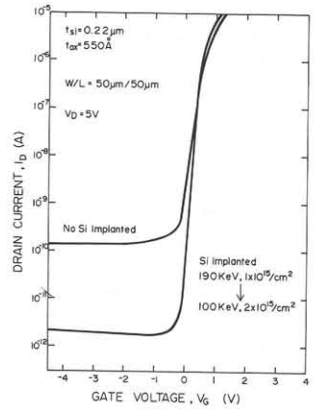

Fig. 3. Typical I_D-V_G characteristics for N-channel SOS transistors.

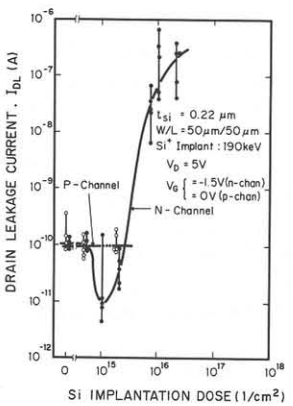

Fig. 4. Drain leakage current as a function of Si ion dose.

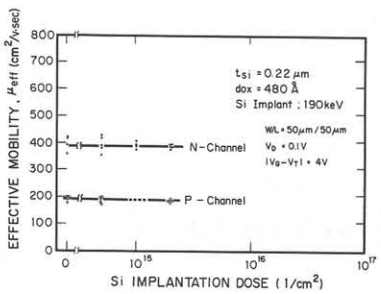

Fig. 5. Effective mobilities as a function of Si ion dose.