B−2−3 Experimental Study of Amorphous Silicon Integrated Circuit

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Recently much attention has been paid to amorphous silicon (a-Si) produced by glow discharge decomposition of silane, since this material exhibits interesting properties such as low localized state densities, high dark resistivity, ability to accept almost any material as a substrate, and so forth. In this presentation, we will describe experimental results about previously proposed a-Si Field-Effect-Transistors (FETs) logic circuits.[1)]

Figure 1 shows an equivalent circuit and a cross sectional view of the fabricated device. We used fused silica as a substrate and molybdenum as a gate electrode because heat-resisting metal and substrate were required for high temperature annealing to improve the CVD SiO_2 gate-insulator quality. Since the driver FET has an n^+- n^-- n^+ structure and positive gate voltage V_{IN} is applied, it operates in an n-channel mode. The n^+ a-Si region blocks the hole injection and therefore prevents the FET from falling into p-channel operation when V_{IN} is low and V_{OUT} is high. Since the load FET has an Al- n^-- Al structure and since negative voltage V_{GG} is applied to its gate, it operates in a p-channel mode.[2)]

The fabrication procedure is as follows. First, molybdenum was deposited by the electron-beam evaporation method on the fused silica substrate. The film thickness was about 4000Å. After patterning Mo, SiO_2 was deposited by low temperature CVD method. The SiO_2 thickness was about 3000Å. Then the samples were annealed at 800°C in N_2 for 30 min. in order to improve the SiO_2 quality. Next, n^- and n^+ a-Si layers were deposited by hot-cathode arc-discharge decomposition of SiH_4 and SiH_4+ PH_3, respectively. Details of this method will be described elsewhere.[3)] Finally Al was evaporated to form the source and drain of the load FET and interconnection lines. Figure 2 shows a microscopic photograph of the integrated inverter. The channel length and width of both the driver and load FET were 10μm and 100μm, respectively.

The transfer curves obtained from the integrated inverter for various V_{GG} values are shown in Fig.3, where V_{DD} was fixed at 40V. The dotted lines are the theoretical transfer curves. The output voltage V_{OUT} changed sharply near the logical threshold voltage (about 15~20V) and ideal step-like transfer curves were obtained. The small-signal gain was about 10. The logical threshold increased with the increase of the absolute value of V_{GG} as previously theoretically predicted.[1)] It is worthy to note that since the hole mobility is about two orders of magnitude less than the electron mobility, large negative voltage V_{GG} was necessary for the load FET to obtain sufficient current.

By interconnecting nine inverters, an integrated ring-oscillator was fabricated. Figure 4 shows the relation between power dissipation per gate and propagation delay time per gate. In this figure V_{DD} was fixed at 100V and V_{GG} was changed. The power-delay product per gate was constant

and about 480pJ. The maximum oscillation frequency was 500Hz. Thus the minimum propagation delay per gate was calculated to be about 110μsec.

In conclusion, we have demonstrated the novel a-Si logic circuit. The static characteristics were confirmed to be very good and the a-Si FET ring-oscillator operated for the first time. We hope that this circuit can be used for self-scan large-area image-sensors[4] and in future three-dimensional integrated circuits.

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References

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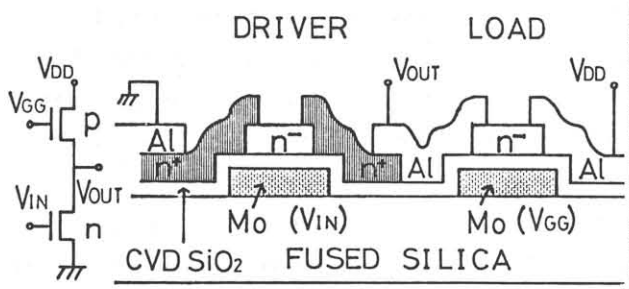

Fig.1
An equivalent circuit and a cross sectional view of the fabricated inverter.

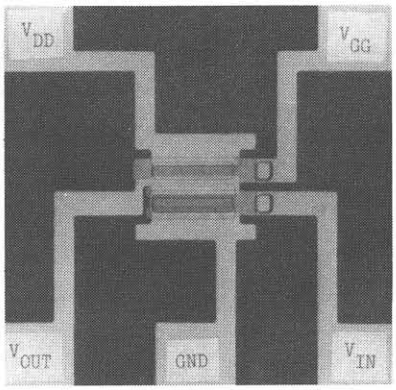

Fig.2
A microphotograph of the inverter.

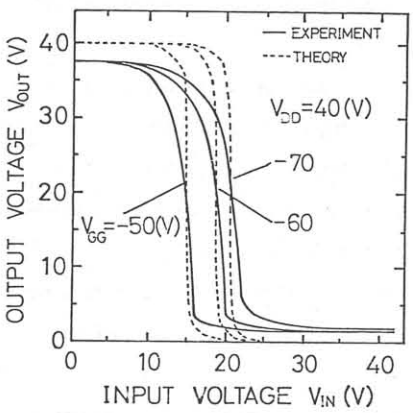

Fig.3
Transfer characteristics of the inverter.

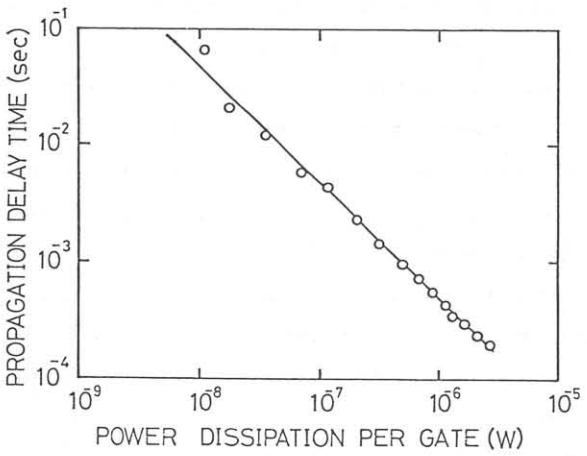

Fig.4
Relation between power dissipation per gate and propagation delay time.