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Josephson Latch Decoder

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For the Josephson high speed computer, decoders used for memory should also be operated as fast as logic elements used in the CPU. Several types of decoders, such as tree, loop and flip-flop decoders[1)-3)], have been proposed hitherto. These decoders are operated under DC power supply condition using current flip-flops and/or selfresetting gates. However, for the high-speed operation, it is useful to construct a decoder with latching gates. In this paper we propose another decoder, which we call a latch decoder. This is constructed from latching gates.

The main features of the latch decoder are simple circuit construction and high speed operation. A logical function of a decoder is generally constructed from AND gates. A two-input AND gate is easily realized with a Josephson junction operated in a latching mode. A latch decoder can be accomplished by using this AND gate as shown in Fig.1. This is an example of a 3bit to 8bit decoder, which includes 14 AND gates in three stages. Three address signals A, B and C and their complement signals are used for selecting one out of eight. For example, when address signals A, B and C are all logic "1" and a decoding start signal I_s is applied, the first of eight output loops is selected in the following sequence. At first the junction J_{11} in the first stage is switched, and then the junction J_{21} in the second stage is switched because the output current of the junction J_{11} and signal B are applied to J_{21} simultaneously. In the third stage, the junction J_{31} is switched to "1". Thus the junction J_{31} makes an output current in the first decoder loop of the third stage. The other junctions remain in the zero voltage state, since at least one of two input signals is logic "0". Consequently, one of eight output decoder loops can be selected corresponding to the states of the input signals A, B and C.

To confirm the operation of this latch decoder, we have fabricated 3bit to 8bit decoder by using 5μm technology. A photomicrograph of the decoder is shown in Fig.2. The chip with a size of $3x3mm^2$ contains 14 AND gates and one test gate. 3-junction interferometer has been used as the AND gate.

Fig.3 shows an operation of the latch decoder. DC current was given as a decoding start signal in this case. The output levels were observed as the voltage across the load resistors. At the first sequence of the operation, address signals A, B and C were all set to logic "1", then the output loop corresponding

to logic function A•B•C was selected. At the second sequence, input signal A was not given, so that all output levels were low. This indicates that interferometers in all stages are operated normally as AND gates. The output voltage in low level is not zero, because of the unexpected contact resistances between counter electrode and control line layers. This can be avoided by careful fabrication or circuit design.

Our latch decoder is simple so that circuit can be made small, and have the potential of high speed operation since interconnections with striplines can be utilized.

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REFERENCES

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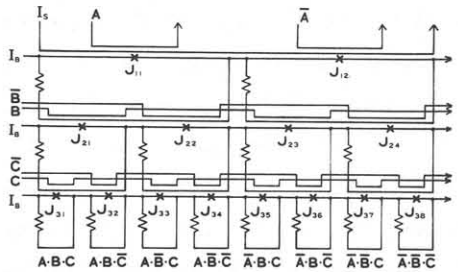

Fig.1 Circuit diagram of the 3bit to 8bit latch decoder.

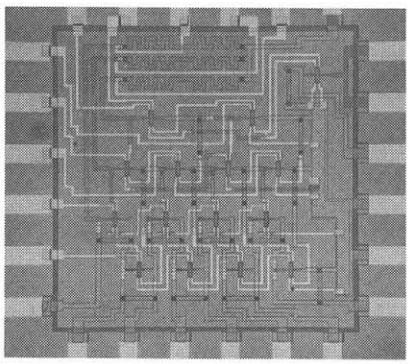

Fig.2 A photograph of an experimental 3bit to 8bit decoder.

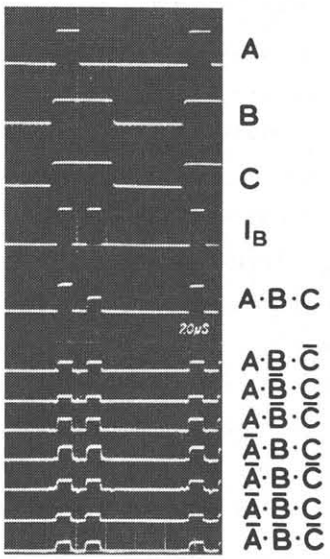

Fig.3 The operation waveforms of the circuit shown in Fig.2. Above four waveforms are given signals A, B and C, and the bias current I_B. The others indicate output voltage waveforms across the load resistor at each decoder loop.