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JOSEPHSON TECHNOLOGY -- A TECHNOLOGY FOR
HIGH PERFORMANCE COMPUTING SYSTEMS

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ABSTRACT

Achievement of high-performance computing systems requires logic circuits with short delays, memories with short access/cycle times, and a very high packaged volume density of these circuits, wherein electrically short signal transmission paths are contained. Computing systems of impressive performance have been designed and made with the Silicon transistor technology as the basis for logic and memory with a variety of packages. To obtain further significant improvement, a considerable number of practical, yet fundamental design and technology problems must be solved. The most fundamental of these is the need to reduce the physical size of the system, in the face of an increasing number of circuits which will comprise that ultra-high performance system. This needed volume circuit density increase is achievable only with improved packaging techniques, reductions of circuit power dissipation levels and/or improvements in powering and cooling techniques. For maximum benefit, such a scale reduction must be accompanied by improvements in raw circuit performance and on-chip densities. While considerable evolutionary improvements in all of these areas can be anticipated for Silicon technology, it is prudent to seek a revolutionary approach, which inherently simplifies the problems and may lead to a quantum jump in performance of computing systems.

The Josephson technology is such a technology. The devices and circuits are of extremely high performance and dissipate little power. For example, Gheewala⁽¹⁾ has reported on a set of experimental logic circuits, fabricated with 2.5 μ m minimum linewidth, with an average logic delay of 36 ps/gate dissipating $\sim 3.4\mu$ W/circuit. Faris, Henkels, Valsamakis and Zappe⁽²⁾ have reported on a 4x1K bit RAM design with an estimated access time of 500 ps and power dissipation of 6 mW. The experiments have been performed using a chip technology described by Huang et al.⁽³⁾ The very low power dissipation permits a simple, dense packaging of chips. Using these package concepts, as described by Brown,⁽⁴⁾ and a 5 μ m minimum linewidth chip technology, Anacker⁽⁵⁾ has estimated, for example, that an IBM 370/168 would have a CPU cycle of ~ 4 ns, and when coupled

with an appropriate Josephson memory hierarchy a performance of ~ 70 Million Instructions per Second, a performance improvement of $\sim X20$ over the existing machine.

It remains to demonstrate that the technology is practical and that projected system performance can actually be achieved. To this end, a small, special-purpose computing system, the Josephson Signal Processor (JSP), will be designed and constructed. The major architectural and design features of this computer have been described by Tsui⁽⁶⁾.

This paper reviews the development of the Josephson technology and describes recent progress toward the JSP at the IBM Research Laboratories.

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