B－5－1 Panel Discussion

Performance Limitation of Si, III-V and Josephson Junction LSIs

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Introduction

Being associated with a change in the rate of increase of component number per LSI chip, physical, technological and complexity limits of Si LSIs have become people's interest and have been discussed in several papers. On the other hand there is a general belief that judging from materials constants III-V LSIs are expected to operate faster than Si LSIs and from physical principle of operation Josephson junctions are expected to work faster than GaAs FETs.

However, technologies of Si LSIs have progressed rapidly by the past and persistent huge R&D efforts and investment. Japanese VLSI project and American VHSIC project are two example of them.

In consequence Si LSIs are chasing III·V LSIs in speed and the speed of chilled GaAs FETs is found to be of the same order of the speed of Josephson junctions. Of course, small power consumption of Josephson junctions in comparison with that of Si MOSFETs and GaAs MESFETs is an inherent advantage to Josephson junctions and a disadvantage of Si devices is that there is no possibility of visible light emission, and some difficulty to combine Si devices with optical integrated cricuits.

Furthermore materials requirements for Josephson junctions are different from those semiconductor devices with a few exceptions because polycrystalline superconductors are used in most cases in spite that semiconductor technology is based on single crystalline Si or III-V substrates.

Therefore there is no conclusion on the performance limitations of Si, III-V, and Josephson junction LSIs which has been unanimously accepted. It is quite timely and worth while to have comparative discussion on this problem now.

Physical Limits

These are limits determined by the universal physical laws, principles and phenomena, such as the uncertainly principle, the thermodynamical laws and the velocity of light. Statistical fluctuation of dopants is one example of them and is one of the phenomena which limit the minimum size of semiconductor devices. However this does not concern the size limit of Josephson junctions. Therefore some of the effects of universal physical phenomena depend on actual type of devices.

Tunneling gives the minimum size of any kind of devices, including

semiconductor devices and Josephson junction devices. It is a common limitation for operational speed in every integrated circuits that the propagation speed of signal cannot exceed the velocity of light. The physical size of ICs limits the speed of operation.

Technological Limits

Technological limits are related to material constants, devices structure, and fabrication technique. Mobility and saturation velocity of carriers have been frequently referred as speed limiting factors of semiconductor devices, but it is not true for Josephson junction devices. Availability of semi-insulating substrate is one of the factors to judge the speed of LSIs, but its use increases electrostatic coupling between interconnection lines and limits the density of lines and devices on a chip. Possibility of fabricating surface inversion type MISFETs' structure and also CMOS configuration is a factor to be considered in order to lower the power consumption in semiconductor devices and to increase the density of components on a chip. Power consumption is recognized as a fundamental limitation to the size of devices and the density of components on a chip. While the size of devices becoming smaller, the power consumption has become so local that the concept of overaged power consumption and temperature rise are no longer valid.

Capability of fine pattern fabrication has been cited so many times as a technological parameter to determine the minimum size of all kinds of devices. Future prospect of electron beam and ion beam pattern delineation technique and DUV and Xray pattern transfer technique is worthwhile to be discussed.

Scaling-down principle is more easily applicable to MOSFETs than to bipolar transistors. The voltage and current limits in transistors are concerned from the viewpoints of power consumption. Scaling-down principle of Josephson junctions must be explored, because the size of existing Josephson junctions is sometimes larger than that of Si MOSFETs.

Complexity Limits

Complexity is a serious difficulty common to any kind of logic LSIs, and limits the number of components on a chip. Computer assisted design tools and methodologies such as structured design concept and gate arrays must be developed. Recently it has been suggested that the number of external connections from VLSI chip will not be increasing monotonically with the number of components in a chip. This is encouraging to integrate more components on a chip.

This abstract is an overview of topics to be discussed in the panel discussion. Conclusion must be drawn during the discussion.