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C-4-1 Anodic Al_2O_3/InP Interface for Application to Enhancement MISFET's

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Introduction

Recently we have shown by detailed analyses that there exists a fundamental differnce in N_{ss} distribution between GaAs and InP MIS interface[1], indicating the feasibility of n-channel MISFET devices on InP in accordance with some recent works[2,3]. In this paper, we describe a simple process to grow anodically high-quality Al_2O_3 films on InP, and clarify the electronic properties of resultant Al_2O_3/InP MIS interfaces. A succesful demonstration of n-channel enhancement MISFET's on Fe-doped semi-insulating InP is also made with the channel mobility of 300 cm^2/V·sec..

Oxide Formation and FET Fabrication

Anodic Al_2O_3 films were formed by anodization of vacuum-deposited Al films on InP, using the AGW electrolyte[4] with glycol to water ratio of 9:1 by volume. Anodization was performed in the constant-current mode with the current density of 0.2 mA/cm^2. Since the changing point from anodization of Al to that of InP is clearly distiguishable on cell voltage vs. time curve, anodization is stopped when this point is reached. The process becomes self-terminating when Al films on semi-insulating InP are anodized with suitalble current supply electrodes. Important anodization papameters are summarized in Table 1.

ANODIC OXIDATION PROCESS

growth rate (Å/V)	13 -14
formation rate (cm^3/coul.)	6×10^{-5}
resistivity (Ω·cm)	10^{15}
breakdown field strength (V/cm)	$2\text{-}3 \times 10^6$
relative permitivity	8.1 - 8.7
frequency dispersion (100Hz - 1MHz)	below 1 %

Table 1

MISFET's were made on Fe-doped S.I.(100) InP with the resistivity of 3×10^8 ohm-cm. The cross-sectional view of the device is shown in Fig.1. Source and drain contacts were formed by alloying Au-Sn or Al-Sn patterns in H_2. The gate length and width were 10 - 30 μm and 300 μm, respectively.

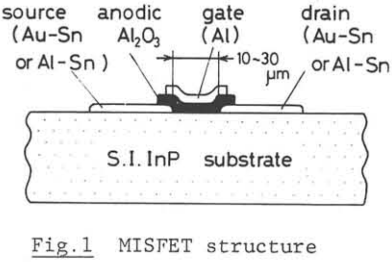


Fig.1 MISFET structure

Properties of Oxide and MIS Interface

Al_2O_3 films thus formed were highly uniform and possessed of excellent dielectric properties as shown in Table 1. Good adhesion to substrate was achieved by applying pre-oxidation annealing of Al films in H_2 at 250°C. AES analyses revealed uniform in-depth profiles with very narrow transition regions.

As compared with the anodic native oxide/InP interface, the present Al_2O_3/InP interface showed superior interface properties. As compared with GaAs MIS interfaces, the frequency dispersion of accumulation capacitance of n-type MIS samples is negligibly small with no reduction of capacitance at low temperatures. On the other hand, inversion capacitance of n-type samples are considerably larger than the theoretical value, and accumulation capacitance of p-type samples show strong frequency dispersion. Fig.2 shows the measured interface state density distribution by Terman's method. DLTS measurements of thermal activation energy of interface states gave 0.64 eV and 0.05 eV for strong inversion and accumulation biases, respectively, for n-type samples, with the values of capture cross-section of the order of 10^{-14} cm^2. Photoionization threshold energy of surface states as measured by the photocapacitance transient spectroscopy technique[5] gave the value of E_c - E_t = 0.7 eV. Thus, the results of dynamic measurements are consistent with the quasi-static ones, and no anomaly as in the case of GaAs MIS,[1] was experienced. This seems to indicate much reduced surface disorders in InP MIS system. Since the surface Fermi level reaches as near as 0.05 eV from the conduction band edge, formation of surface n-channel should be possible.

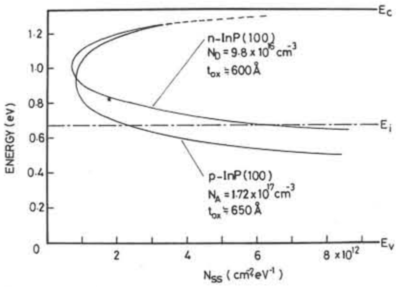
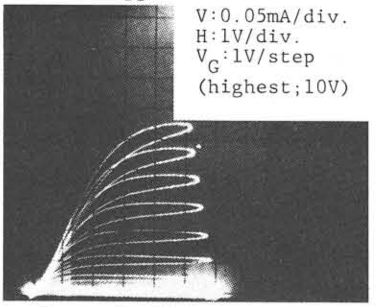


Fig.2 N_{ss} distribution

FET Characteristics

Fig.3 shows the I-V characteristic of an anodic Al_2O_3/InP n-channel MISFET fabricated on S.I. substrate. Hysteresis in I-V curves seems to correspond to small C-V hysteresis in MIS diodes, and indicates slow electron trapping process at the interface. I_{DSS} follows the square law vs. V_G for small V_G. Estimated channel mobility is shown in Fig.4 with the maximum of 300 $cm^2/V \cdot sec$.. Further improvements seems possible by improving interface properties and using substrates of higher quality.



V_{DS} - I_D CHARACTERISTICS
Fig.3

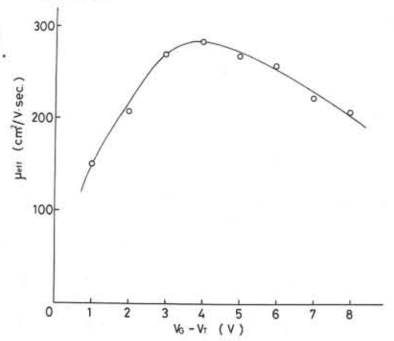


Fig.4 Channel mobility

References 1.Hasegawa et al, IEEE Trans.ED-27 ('80)1055 2. Meiners et al, Electron. Lett.15 ('79)578 3. Kawakami et at, Electron. Lett.15 ('79)743 4. Hasegawa et al,J.Electrochem.Soc. 123('76)713 5.Hasegawa et al, Proc.15th Int.Conf.Phys. Sem.(Kyoto,'80) 1125.