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A 1K bit Associative Memory LSI

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A 1K bit associative memory LSI has been fabricated. This LSI is designed to carry out all of the functions necessary to realize a high performance data search system. As well as a data search function, a retrieval function to process searched out data is implemented on the chip, so as to realize a self-operative, large-capacity associative memory. Furthermore , a search function for similar data is implemented so as to be able to use the associative memory over a wide range of applications.

There are some serious problems in developing an associative memory LSI: (1) The large number of terminals for searched out data processing must be reduced; (2) A function to extend the length of searched for data beyond the LSIs must be realized to achieve a satisfactorily large search system. In order to reduce the number of terminals, the retrieval function has been implemented on the chip, so that multiple searched out data can be resolved and the selected data can be put out one by one. For extending the data length, lengthy data units are divided and stored under the same word in different LSIs. In such cases, data search operations are carried out by communication of word address data.

A new memory cell circuit has been designed to facilitate the search for similar data. A drawing of the circuit is shown as Figure 1. A cell array composed of these circuits allows calculation of the number of non-coinciding bits (Hamming distance) between the stored data and interrogative data with word-parallel operation.

The associative memory LSI consists of a retrieval function unit and associative memory cell array. A block diagram is shown in Figure 2. The LSI decodes input instructions and carries out operations , such as 'Write', 'Search', 'Multiple Response Resolve', and 'Read'.

A microphotograph of the fabricated 1K bit associative memory LSI is shown in Figure 3. The memory is composed of 64 words by 18 bits. Figure 4 shows an example of the input/output signal waveforms. These indicate that the searched out data are retrieved every two cycles, and a high rate of throughput is realized. The chip size is 4.1 mm x 4.95 mm. Minimum

cycle time is 100 ns. The features of the associative memory LSI are summarized in Table 1.

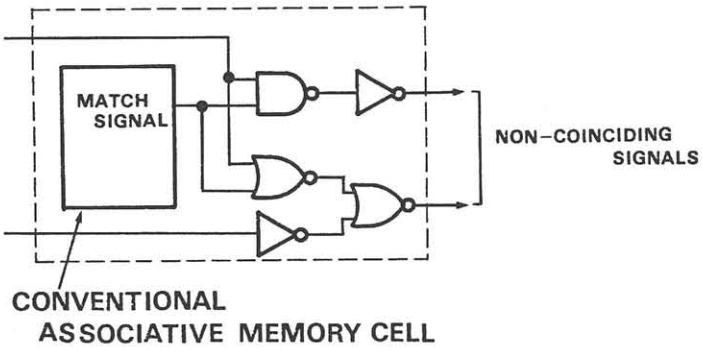

FIGURE 1-Associative memory cell circuit.

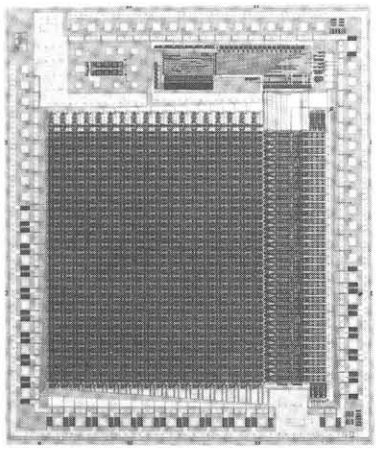

FIGURE 3-Microphotograph of the chip.

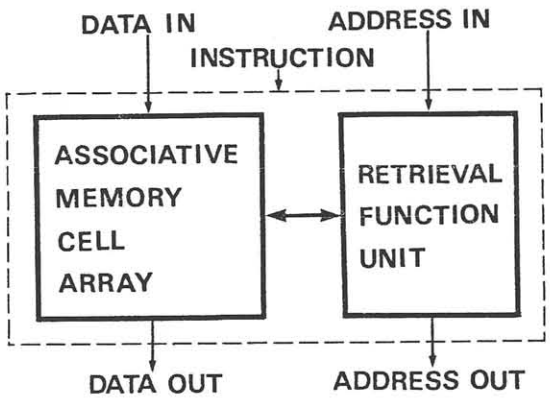

FIGURE 2-Associative memory block diagram.

WORD ORGANIZATION	64w x 18b
CHIP SIZE	4.1 mm x 4.95 mm
CYCLE TIME	100 ns min.
SUPPLY VOLTAGE	5 V
POWER DISSIPATION	1.2 W
I/O INTERFACE	TTL
NUMBER OF PINS	62
PROCESS TECHNOLOGY	2 μm n-channel E/D MOS Double layer Al interconnection

TABLE 1-Typical characteristics of 1K associative memory.

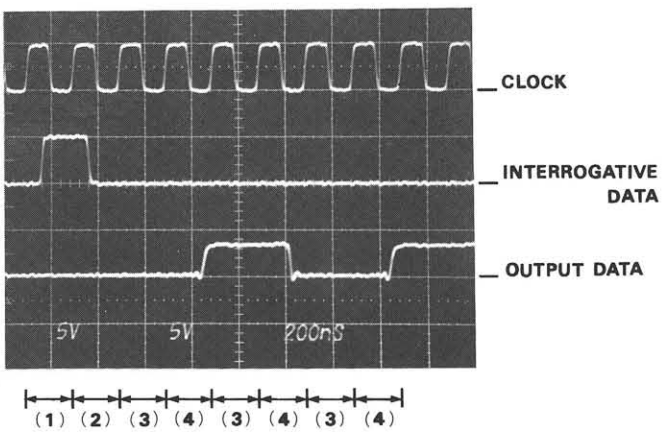

FIGURE 4-Input/output signal waveforms.