A — 2 — 3 New dynamic RAM cell combined with Hi-C structure

H.Ozaki, K.Shimotori, K.Fujishima, S.Satoh, and T.Nakano
LSI Research & Development Lab.,Mitsubishi Electric Corp.
4-1 Mizuhara, Itami, Hyogo, 664, Japan

According as the progressing of the fine patterning, the problem has occurred that the active area is decreased by the lateral oxidation under the nitride masks in the LOCOS process, so called bird's beak. Particularly, in the dynamic RAMs beyond 256K bits, the decrease of the effective active area of the storage capacitor caused by the bird's beak is pronounced. Coping with this problem, the new process technology has been announced.[1)]

In this paper, a new dynamic RAM cell combined with the Hi-C structure will be proposed which is fabricated by using the conventional LOCOS process, and moreover, reduces the influence of the bird's beak.

The structural comparison of the new cell and the conventional one is shown in Fig.1. The storage capacitors of the both type cells consist of the doubly ion-implanted Hi-C structure[2)] and the MOS capacitor. In the conventional cell, the active region forming the storage capacitor is isolated from the adjacent cell by the thick SiO_2 layer (0.75 μm). On the other hand, in the new cell, it is isolated by the p^+ region formed by the p-type implant of the Hi-C structure. As the result, the new cell makes it possible to prevent the decrease of the active area caused by the bird's beak in this region.

The storage capacitance of the both type cells was measured by the test device. The equivalent circuit of this device is shown in Fig.2. The gate oxide thickness of the test device was 28 nm and the n- and p- type implant dose for the Hi-C structure were 3×10^{13} cm^{-2} and 7×10^{12} cm^{-2}, respectively. The output waveforms through the analog buffers of the test device are shown in Fig.3. This photograph indicates that the storage capacitance of the new cell is 13 % larger than the conventional one's. This result shows the good agreement with the calculated result assuming that the loss of the active area by the bird's beak is 0.5 μm.

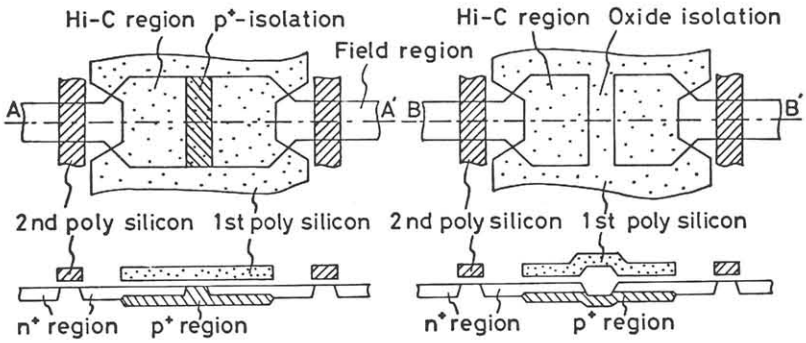
In the dynamic RAM cell, the high breakdown voltage and the low leakage current between each cell are required of a high yield and wide operating margin. In both type cells, when the cell plate was applied at 0 V, the breakdown voltage against the adjacent cell was about 12 V, which was restricted by the junction breakdown of the Hi-C structure. But in the new cell, because

SiO_2 layer on the isolation region is thin, adjacent two storage capacitors showed the transistor action at the relative low cell plate voltage. The I - V characteristics of this transistor is shown in Fig.4. The threshold voltage (V_T) of this parasitic transistor was 2.1 V, when the back bias voltage(V_{BB}) equaled to -3 V, corresponding to the operating condition of RAM. On the other hand, V_T of the transfer transistor of the cell was 1.0 V at V_{BB} = -3 V. Therefore, when the cell plate is applied at 0 V (the grounded cell plate), the leakage current between cells will be ignored, compared with that of transfer transistor.

In conclusion, the new cell is suitable for the dynamic RAMs using the Hi-C structure, the grounded cell plate, and the back bias, and it gives 13 % larger capacitance than the conventional one.

Reference

1) K.Kurosawa et al; Technical Digest, IEDM, 384 (1981)
2) M.Yamada et al; Technical Digest, IEDM, 578 (1980)



New Cell Conventional Cell

Fig.1 Memory cell structure of new cell and conventional one

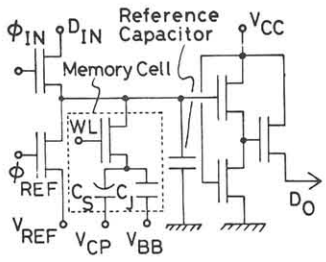


Fig.2 Equivalent circuit diagram of test device for C_S measurement

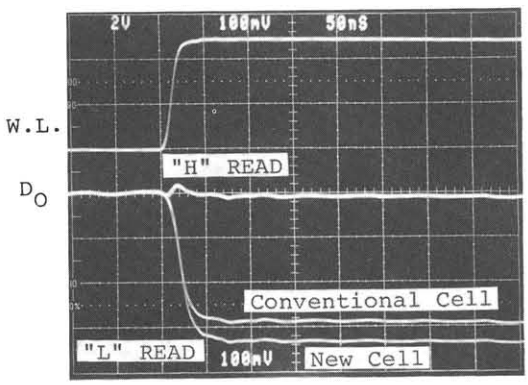


Fig.3 Output waveforms of test device

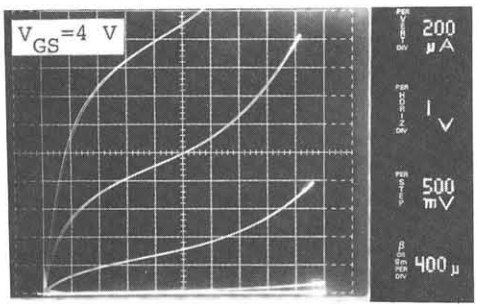


Fig.4 I_D - V_{DS} characteristics for parasitic transistor with L = 1.6 μm of isolation region (V_{BB} = -3 V)