

## A-2-4 Hot-Electron Trapping Effects of Short Channel 64 K dynamic MOS RAM

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The channel hot-electron trapping is one of the serious problems in scaled-down dynamic MOS RAM's. This effect causes a degradation of the electrical characteristics in the MOS transistor such as a threshold voltage ( $V_{TH}$ ), which results in a performance degradation of MOS RAM's. In this paper, an empirical approach for circuit designs is presented on the channel hot-electron trapping effects of actual 64 K dynamic MOS RAM's.

Fig.1 and Fig.2 show the access time and address hold time shift, respectively, of the 64 K RAM's with short channel length  $L_{eff}=1.9 \mu m$ . The shift of the access time and column address hold time occurred while the row address hold time has not changed appreciably. This fact implies that some critical paths are sensitive to the channel hot-electron effects. Fig.3 is a delay channel of the  $\overline{RAS}$  access time before the long term stress and after that, respectively. The driver circuits associated with the sense amplifier, column address buffer, and output buffer mainly contribute to the access time shift. Those driver circuits have almost the same circuit configuration, as shown within the dotted line of Fig.5. Therefore, from the viewpoint of circuit designs, it is important to investigate the behavior of the typical driver circuit.

In order to evaluate the  $V_{TH}$  shift of each MOS transistor in the typical driver circuit, an n-channel test device, shown in Fig.4, was fabricated on p-type (100), 20 ohm-cm substrate. Fig.5 shows the equivalent circuit of the device, which consists of the actual driver circuit and  $V_{TH}$  measuring MOS transistors ( $Q_M$ 's). The transistors  $Q_M$  are added to minimize the stray capacitance of the internal nodes ( $N_1-N_6$ ) in the operating mode. During the operating mode, the device functions as a realistic dynamic inverter by maintaining the level of  $V_{TM}$  low. On the other hand, during the  $V_{TH}$  measuring mode,  $V_{TM}$  is kept high to connect the internal nodes with the external terminals ( $E_1-E_6$ ). The long term stress experiments, where both modes repeated alternately, were executed with the dynamic burn-in system. Table I lists the channel hot-electron  $V_{TH}$  shift after 65 hours under the stress condition of  $V_{CC}=9.5$  V and  $T_a=10$  °C. Several MOS transistors ( $Q_2, Q_6, Q_8, Q_{11},$  and  $Q_{12}$ ) experienced higher shift than others. From the recent studies on the hot-electron trapping of MOS transistors<sup>(1)</sup>, it is evident that the  $V_{TH}$  shift increases abruptly with the drain bias, and that under the constant drain bias, the  $V_{TH}$  shift increases with the decrease of the gate bias, i.e., the channel

hot-electron trapping becomes more serious at  $V_{GS}$  (gate-to-source voltage)  $< V_{DS}$  (drain-to-source voltage). On the basis of the above model, the transistor operating point was analyzed using  $V_{GS}-V_{DS}$  trajectories by the computer circuit simulation. The specified MOS transistors operating under the bias condition of  $V_{GS} < V_{DS}$  just correspond to those which suffered higher  $V_{TH}$  shift. Using the  $V_{TH}$  shift of those transistors, the simulated access time shift of the 64 K RAM's shows a good agreement with the experimental value.

In conclusion, it has been verified that the performance degradation of the short channel dynamic MOS RAM's is mainly attributable to the specified MOS transistors which operate under the bias condition of  $V_{GS} < V_{DS}$ . Such a sensitive transistor has been predicted by analyzing the  $V_{GS}-V_{DS}$  trajectories through the empirical MOS transistor model developed by the long term stress experiments. Reference 1) H. Matsumoto, et al., IEEE Trans. Electron Devices, ED-28(1981)923.

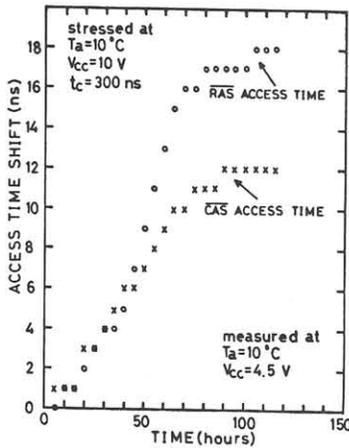


Fig.1. Access time shift of 64 K RAM with  $L_{eff}=1.9 \mu m$ .

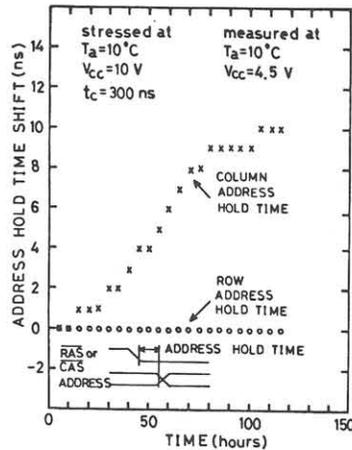


Fig.2. Address hold time shift of 64 K RAM with  $L_{eff}=1.9 \mu m$ .

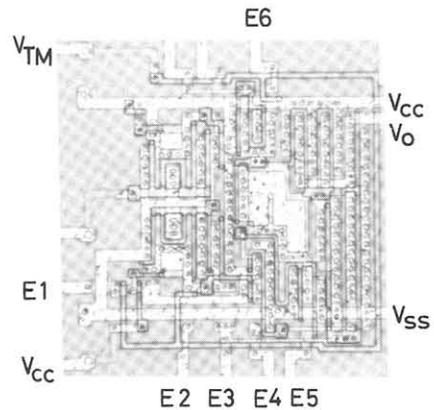


Fig.4. Photomicrograph of test device.

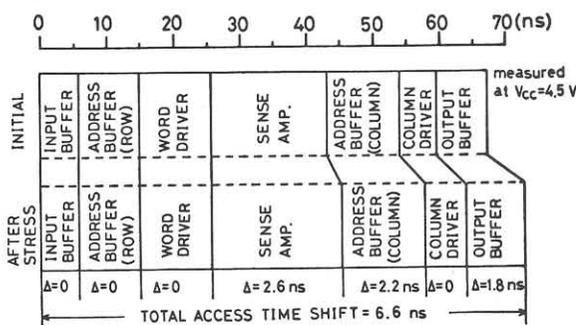


Fig.3. Delay channel of  $\overline{RAS}$  access time shift after 48 hours' stress.

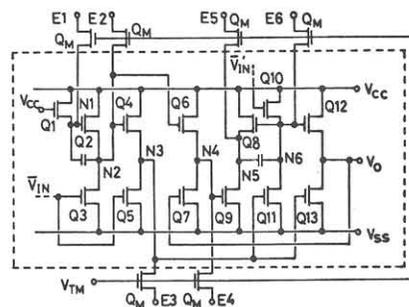


Fig.5. Equivalent circuit of test device.

Table I. Channel hot-electron threshold shift after 65 hours' stress (See Fig.5)

MOS transistor	$L_{eff}$	$\Delta V_{TH}$	MOS transistor	$L_{eff}$	$\Delta V_{TH}$
$Q_1, Q_3, Q_4, Q_5,$ $Q_7, Q_9, \text{ and } Q_{10}$	$1.9 \mu m$	0.00	$Q_8$	$1.9 \mu m$	0.93 V
$Q_2$	$1.9 \mu m$	0.26 V	$Q_{11}$	$2.4 \mu m$	1.24 V
$Q_6$	$1.9 \mu m$	1.97 V	$Q_{12}$	$1.9 \mu m$	0.17 V
			$Q_{13}$	$1.9 \mu m$	0.01 V