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A—2—5 Redundancy Techniques for Dynamic RAMs

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I INTRODUCTION

This paper describes redundancy techniques designed for a 256K dynamic RAM with poly-Si fuses as an electrically programmable ROM. Special attention is paid for the following items;

(1) Optimization of a size of redundancy, (2) Device structure of poly-Si fuses, (3) Fusing mechanism and modeling, (4) Reliability consideration, (5) Experimental results of the yield improvement factor.

II OPTIMUM SIZE OF REDUNDANCY

A size of redundancy required to obtain the maximum yield can be given by considering a trade-off between the increase in the yield with increasing a size of redundancy and the decrease in the yield with the increased chip size due to redundancy[1]. Fig.1 shows the calculated result of the yield improvement factor versus the number of redundant lines(rows/columns). It is clear that the maximum yield improvement for the RAM can be attained at around four redundant lines.

III DEVICE STRUCTURE AND FUSING CHARACTERISTICS

Poly-Si fuses were chosen as electrically programmable ROMs[2] for simplifying processing and testing. The device structure of a poly-Si fuse is shown in Fig.2. The characteristics of this structure is two fold;First,a first level poly-Si is used,thus enabling the use of a polycide or a metal as a gate material for high speed RAMs. Second,a two step etching process is used to remove the PSG and the final passivation layer for passivation holes. This structure prevents the exposure of the PSG,designated as (a) in Fig.2, thus attainning high reliability .

Fusing characteristics have been studied and a one-dimensional thermal equation is developed to determine the fusing current and time. For the steady-state,the fusing current I_f is obtained as follows;

$$I_f = \sqrt{\frac{T_{melt}\cdot\lambda_{SiO_2}}{\ell_{LOCOS}}}\left(\frac{1}{R}\sqrt{\frac{\rho_{Si}}{t_{Si}}}\right)\frac{\ell}{\sqrt{1-\frac{\sinh(\frac{1}{2}\sqrt{\alpha}\ell)}{\sinh(\sqrt{\alpha}\ell)}}},\quad \alpha = \frac{\lambda_{SiO_2}}{\lambda\cdot\ell_{LOCOS}\cdot t_{Si}}$$

Where, T_{melt} is the melting point of Si, λ and λ_{SiO_2} are the thermal conductivity of Si and SiO ,respectively, ℓ is the fuse length,R is the resistance of the fuse, ρ_{Si} is the resistivity of poly-Si, t_{Si} is the fuse thickness, ℓ_{LOCOS} is the thickness of the LOCOS SiO_2. Fig.3 shows the comparison of I_f between the calculated and experimental results. The agreement between the calculation and the experiment

is quite satisfactoy and this equation has been used for determining device parameters of poly-Si fuses and the size of transistors for blowing fuses. More detailed discussion and the time dependence of fusing will also be presented.

V 256k DYNAMIC RAM WITH REDUNDANCY

Fig.4 shows a photograph of a 256K dynamic RAM test device with redundancy discussed above. Fig.5 shows the experimental results of the yield improvement factor[3]. The yield is improved by a factor of 5-10,thus showing that redundancy will be prerequisite to future high density memories.

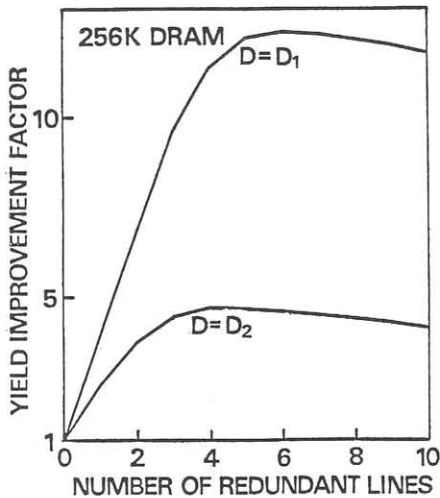

Fig.1 Number of redundant lines vs. yield improvement factor

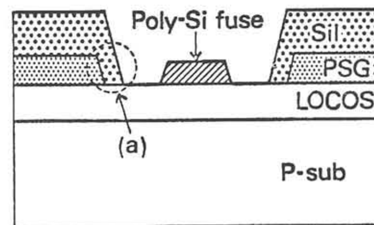

Fig.2 Device cross section of a poly-Si fuse

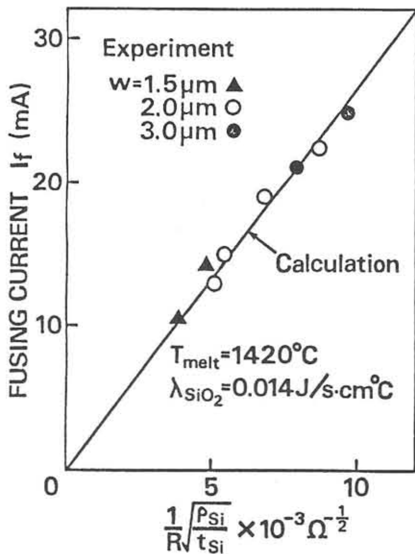

Fig.3 Comparison of If between the experiment and the calculation

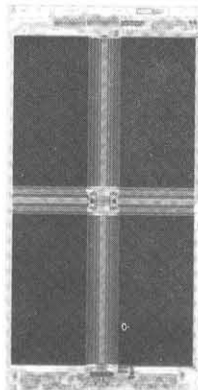

Fig.4 Photomicrograph of a 256K dynamic RAM

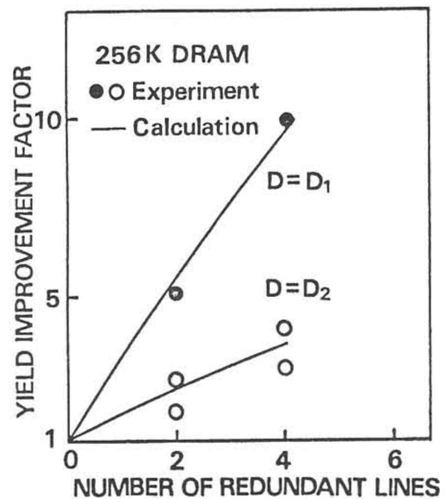

Fig.5 Experimental result of yield improvement factor

V REFERENCES, [1] T.Mano et al,ISSCC80,Dig.Tech.Papers,P.234,1980, [2] P.K.Wallace et al,Electronics/March 27,P.147,1980.[3] J.F.M.Bindels et al,ISSCC 81,Dig. Tech. Papers,P.82,1981.