A — 2 — 6 Soft-Error Analysis Of Fully Static MOS RAM

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A static MOS RAM cell with polysilicon resistive load (>50Mohm) has been analyzed with respect to an alpha-particle induced soft-error phenomenon. The cell design for minimizing the soft-error rate has been obtained from the analysis of effective critical charge Q_{crit}.

The static RAM cells having high impedance loads shown in Fig.1 suffer from the soft-error problem as do the dynamic RAM cells. The model of soft-error process is expressed in the V1-V2 plane as shown in Fig.2, where Γ_0 (Γ_0'; $R1 \cdot C1 \neq R2 \cdot C2$) is the line which indicates the unstable equilibrium points. The points P1 and P2 indicate the stable states when Tr.1 and Tr.2 are in the off-state. The stable points are Q1 and Q2 in a read out operation. The cell state is originally at the point I in Fig.2. When enough electrons are injected into a storage node which is in the high voltage level V_H, the storage node voltage is reduced and the cell state moves from the point I to P2 through the point A, B and C. The voltage of "L" storage node is also lowered in the amount of $V_{\alpha L}$ by the electron injection or C-coupling between the "H" and "L" storage node. The effective critical charge Q_{crit} which is defined as the amount of collected charge in "H" storage node when the soft-error occurs is written as follows;

$$Q_{crit} = (C1+C3) \cdot (V_H - Vth) + (C1 + \frac{C2 \cdot C3}{C2+C3}) \cdot (Vth - V_\Gamma + V_{\alpha L} \cdot (1 - \frac{V_\Gamma}{Vth})) \quad \text{-----} \quad (Eq.1),$$

where V_Γ is the voltage V1 at the cross point of Γ_0' and x-axis. ($V_\Gamma = 0$; $R1 \cdot C1 = R2 \cdot C2$) A tiny compensation current (<0.1μA) through the polysilicon resistor is neglected.

The value of V_H is kept to Vcc in the data retention mode. However, in the active mode, V_H lowering is unavoidable after not only the write operation but also the read operation, especially, in the high density and high speed design. Every time a row select line is charged up, V_H falls to the stable level V_R in the read out operation and rises to Vcc level with a large time constant. This V_H lowering reduces Q_{crit}, consequently enhances the soft-error rate in the shorter cycle time operation. Fig.3 shows the cycle time dependence of the error-rate. The error-rate is decreased and saturated with increasing the cycle time. In practical operations, the error-rate increases with higher R_H, but it does not depend on R_H in the long cycle operation. Fig.4 shows the dependence of the error-rate on Vcc. The error-rate is decreased with increased Vcc. The error-rate has a strong dependence on Vcc for the lower R_H or the longer cycle time. It is less dependent on R_H in the longer cycle time range.

Eq.1 also suggests the relation ship between the cell layout and the error-rate. The increase of V_{α_L} results in the increase of Q_{crit}. On the other hand, the imbalance of two pull-up resistors increases V_Γ and cancels the V_{α_L} effect so that Q_{crit} is reduced, effectively. From these consideration, a high tolerance cell against the soft-error has been designed according to the following items ; (1) Individual two storage N^+ regions were placed closely, which enlarged V_{α_L}. (2) The pull-up devices were formed on a flat field oxide region, which balanced two pull-up resistors. (3) The area ratio of N^+ storage region to other N^+ region were made as small as possible, which reduced the collection efficiency of electrons. Fig.5 shows the comparison of the error-rate between the present cell and another cell[1] which fabricated by double polysilicon technology and had about twice as large as storage capacitance. The alpha-particle endurance of present cell has been improved 10 to 100 times in spite of the storage capacitance disadvantage.

The experimental results show a good agreement with the above mentioned model for the soft-error of the static MOS RAM.

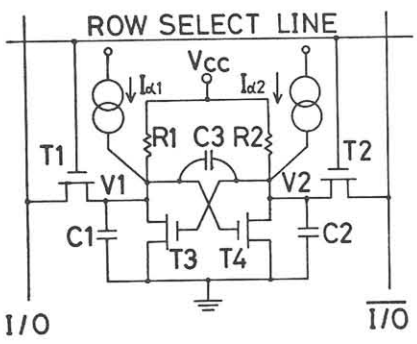

Fig.1 Memory cell circuitry.

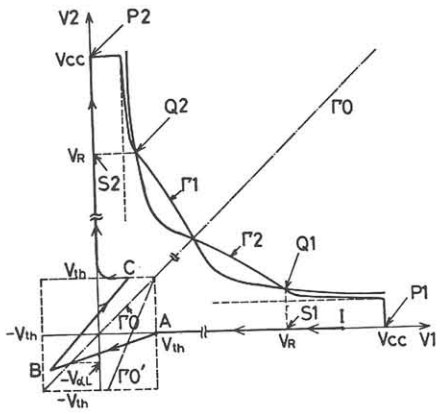

Fig.2 V1-V2 plane which shows states of memory cell.

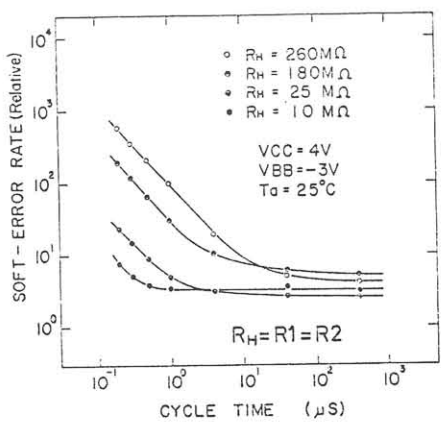

Fig.3 Cycle time dependence of soft-error rate.

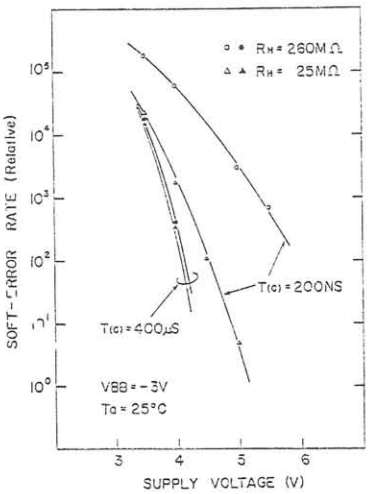

Fig.4 Vcc dependence of soft-error rate.

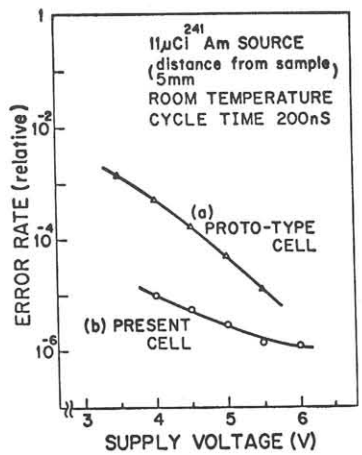

Fig.5 Comparison between two kinds of cells.

Ref. 1) K.Anami et al. ; ISSCC DIJEST OF TECHNICAL PAPERS, p.250-251; Feb.,1982.