A — 3 — 1

High Voltage Dielectric Isolated IC Technology

Y. Sugawara, T. Kamei, Y. Hosokawa, S. Okuhara, I. Oohinata

Hitachi Research Laboratory and Totsuka works, Hitachi, Ltd.

Hitachi and Yokohama, Japan

EPIC (Epitaxial Passivated Integrated Circuit) process is a conventional dielectric isolation technique which was developed about fifteen years ago. In spite of its excellent characteristics including high isolation voltage, low parastic capacitance and no latch up actions, it has been applied to a relatively limited area because of its rather complicated process. Recently, applications of the EPIC process to telecommunication ICs, such as crosspoint switches and subscriber line interface circuits[1,2], which require high voltage, high noise capability and high accurancy, have started.

However, the dielectric isolation has some problems. One is that the breakdown voltage, BV, of elements in the dielectric isolated island which are affected by the potential of the polysilicon substrate. This results in a decrease of BV when high voltages, such as lightening surges and ringer signals, are applied to ICs. The other is that minority carriers are recombined at an interface between the isolation oxide and the single crystalline silicon island. This results in a decrease of the lateral pnp transistor h_{FE} value and an increase in the thyristor FVD.

New techniques were developed to solve these problems. In the first place, a channel stopper structure with n^+ buried layer shown in Fig. 1(a) was newly designed in order to eliminate the dependence of BV on the substrate potential, which also acts to eliminate the recombination of minority carriers at the interface. Fig. 1(b) shows a conventional channel stopper structure without n^+ buried layer.

Fig. 2 shows the calculated maximum electric field E_{max} vs. the oxide thickness for the 4μm junction depth diodes shown in Figs. 1(a) and (b), which have a field plate along with the channel stopper to realize high voltage. The E_{max} in the structure with the buried layer is lower than that of the conventional structure, therefore it achieves a higher BV for the same oxide thickness.

Fig. 3 shows the calculated BV of the structure with the buried layer as a function of fixed charge density Q_{SS} in passivation oxide. It is evident that Q_{SS} must be controlled within a limited range in order to obtain the required BV and that this range becomes smaller, as the junction depth becomes shallower. Therefore, a technique, which is able to control the Q_{SS} by controlling temperature and atmosphere of final heat treatment in LSI fabircation process, was developed. The BV is limited by the electric field at the place b and increases with increasing t_1 when the Q_{SS} is lower than the peak point of the curve in Fig. 3. Therefore, the wider Q_{SS} range can be obtained by the increase of the t_1. Calculated relationships as shown in Fig. 3 were confirmed experimentally and high BV devices were realized. These results will be presented in a detailed manuscript now being prepared.

Using above techniques, npn transistor ($BV_{CBO} \geq 350V$, $h_{FE} \simeq 100$) and pnp transistor ($BV_{CBO} \geq 350V$, $h_{FE} \simeq 10$) were developed with 3.5μm junction depth, and both lateral thyristor and gate turn-off lateral thyristor of $BV > 400V$ were also developed with 18μm junction depth.

The dependence of the device characteristics on the distance from the junction to the isolation oxide was

studied, and it was found that lateral pnp transistor h_{FE} depended on the distance strongly. Therefore, pnp transistors in current mirror circuits and comparators were designed under the consideration of h_{FE}'s distance dependence. On the other hand, resistance ratios of diffused resistors were rarely dependent on the distance and a high accurancy of resistance $\leq \pm 1.0\%$ was achieved.

To avoid the expensive two level metallization and to decrease the chip area, a new crossunder technique between high voltage circuit interconnections was developed, in which the n^+ buried layer of the isolated island was utilized as the crossunder interconnection. All of these techniques were applied to the development of the 350V switching ICs and the 250V analog IC together with newly developed circuit techniques, which were the exclusive control technique between two thyristors and the interruption technique of large current 500mA etc. Fig. 4 shows a photograph of 350V, 250mA switching IC chip for telecommunications.

References

1) T. Kamei, "High Voltage Integrated Circuits for Telecommuncations," IEDM Technical Digest, p.254 ; Dec., 1981.

2) K. Kawarada et al, "High Voltage Subscriber Line Interface LSIs," ISSCC Digest of Technical Papers, p.202-203 ; Feb., 1982.

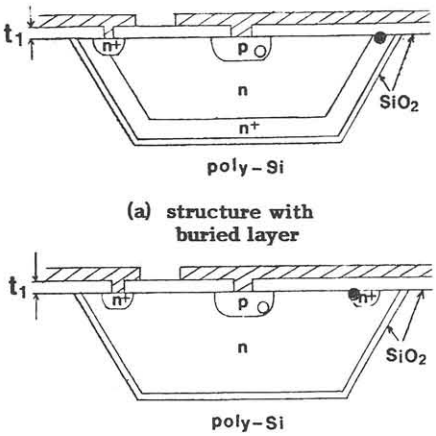

Fig. 1 Structures of channel stoppers.

○ shows place a, ● shows place b.

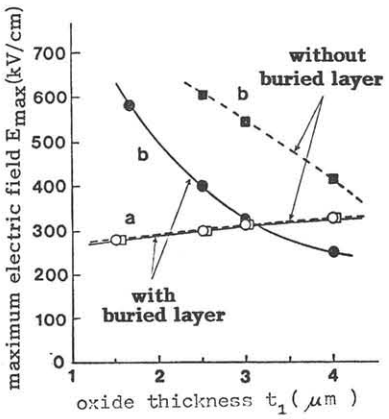

Fig. 2 Maximum electric field E_{max} vs. oxide thickness t_1 of 4μm junction depth diodes. (applied voltage : 400V)

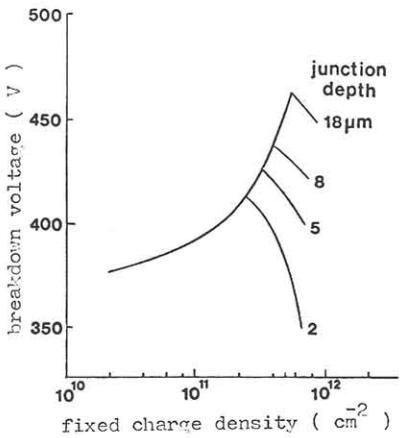

Fig. 3 Breakdown voltage vs. fixed charge density Q_{SS} for the diodes of the structure with the buired layer.

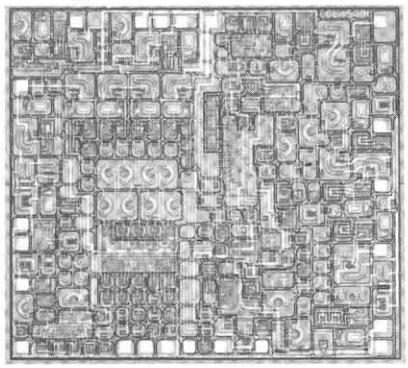

Fig. 4 A photograph of the 350V, 250mA switching IC.