A - 3 - 3 Compatible High and Low Voltage CMOS Devices using SIMOX Technology

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Integration of high and low voltage CMOS devices has been recently achieved using bulk MOS technology and SOS technology (1). However, bulk MOS technology has several problems, such as latch up and the decrease of drain current due to backgate bias effect. SOS technology has problems of drain leakage current and high substrate cost. This paper describes a new type compatible high and low voltage CMOS devices, such as a current mirror and an operational amplifier using buried channel MOS FET and SIMOX isolation technology.

Figure 1 shows a cross sectional view of the high voltage (HV-) and the low voltage (LV-) devices. Silicon island height \( t_{Si} \) is 3000 \( \AA \), gate oxide thickness is 700 \( \AA \) and channel impurity concentration \( N^+ \) is \( 1.5 \times 10^{15} \) cm\(^{-2} \). Both high and low voltage devices are easily integrated on a single chip by controlling offset gate length \( L_o \). A 180 V drain breakdown voltage for N-ch HV-MOS(2) and a 250 V for P-ch HV-MOS(2) were obtained with \( L_o = 20 \) \( \mu \)m. Typical LV-CMOS \( I_D - V_D \) characteristics are shown in Fig.2. The top is for P-ch with \( W/L = 120/30 \) and the bottom is for N-ch with \( W/L = 30/30 \), respectively.

Figure 3 shows buried SiO\(_2\) characteristics formed by SIMOX technology. Both buried SiO\(_2\) thickness and breakdown voltage are proportional to \( \phi_{16O^+} \) dose. The electric field strength for breakdown is calculated to be about 7 MV/cm, which is the same as that of the thermally grown SiO\(_2\).

Figure 4 shows drain current characteristics versus substrate voltage. The devices made by a bulk MOS process are sensitive to substrate voltage \( V_{sub} \). Moreover, \( V_{sub} \) can not be applied to the forward bias for the substrate to source P-N junction. In devices made by SIMOX technology, a layer shielding the electric field can be easily formed on the buried SiO\(_2\) layer by selecting a suitable \( 16O^+ \) implantation parameters(4), such as 150 KV implanting energy and \( 1.8 \times 10^{18} \) ions/cm\(^2\) dose. This layer makes the drain current characteristics insensitive to the substrate voltage. The devices formed by SIMOX technology are suitable for use as analogue devices, such as current mirrors and operational amplifiers, especially for complementary use and high voltage use.

Figure 5 shows MOS current mirror characteristics. The threshold voltage variation to the substrate bias is greatly suppressed by using the SIMOX substrate. Matching errors in the low current region are dominated by the variation in the threshold voltage and are inversely proportional to the drain current. In the high current region, matching errors are dominated by the variations in
channel length and width. Both in low and high voltage current mirrors, 0.5% of matching errors in 10 μA drain current are obtained without any compensation circuits which are necessary for bipolar current mirrors.

Figure 6 shows two stage operational amplifier characteristics. A bulk MOS operational amplifier has suffered from a low open loop voltage gain due to back-gate bias effect, so compensated load schematics have been proposed (5). Devices made by SIMOX technology have a high open loop voltage gain of 60 dB and a good phase margin without any compensation load circuits and capacitor Cg. In addition, low power dissipation of 1 mW at +5 V is obtained.

References
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Fig. 1 Cross sectional view of the high and low voltage devices

Fig. 2 Low voltage CMOS ID-VD characteristics

Fig. 3 Buried SiO2 characteristics using SIMOX technology

Fig. 4 Substrate voltage dependence of drain current, ID0 is the current at Vsub = 0

Fig. 5 MOS current mirror characteristics

Fig. 6 Two stage operational amplifier characteristics