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A New Linearity Error Correction Tecnology for A/D and D/A Conversion LSI

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To realize high precision monolithic A/D and D/A converters, digital trimming technologies[1], [2] have been investigated instead of laser trimming technologies. A new error correction technology LECS(Linearity Error Correction by Digital Code Shift) utilizing a fully digital processing and a two stage weighted capacitor array(C-C array)[3] is proposed. This technology has an advantage that is significant reduction in required matcing tolerance for weighting network components and number of high precision analog circuits. This paper describes the basic correction principle, its effectiveness and a 14 bit accuracy A/D and D/A converter configuration based on this principle.

Figure 1 shows the correction technology principle for a successive approximation A/D converter. In the figure, the broken line indicates an ideal local DAC characteristic and a solid line shows the original local DAC characteristic before error correction. The conversion error is caused mainly by higher order bit component mismatching. For convenience' sake, the DAC is divided into two portions. One is the higher order portion, called MDAC, and the other is the lower order portion, called LDAC. To achieve error correction, this original DAC should have a redundancy, in that analog output always decreases at MDAC input code changing point. Using the redundancy, the correction can be performed by shifting the input code. This can be easily done by digital add/subtract, so as to coincide with the ideal characteristic.

The original DAC configuration using a C-C array, as shown in Fig. 2, can realize the redundancy by setting the proper Cc value. The DAC is implemented by a CMOS LSI technology with precise analog circuits.

Figure 3 shows the correction effect, that is, required component matching tolerance vs. probability for 14 bit linearity realization, obtained by the statistical error analysis. Conditions to obtain linearity by the LECS technology are as follows. LDAC linearity and negative transition in C-C array transfer characteristic are necessary at every MDAC input changing point, as shown in Fig. 1. These conditions mean that the optimum bit assignment for MDAC and LDAC and Cc value are derived to obtain high yield. Figure 3 shows significant reduction in matching tolerance,

compeared with non-trimmed C-C array and C array. This means that total capacitor value can be reduced, whereby chip area saving and high speed conversion are achieved.

Using LECS technology, the 14 bit 1 chip A/D and D/A converter LSI has been designed. The blockdiagram is shown in Fig. 4. The Code Shifter for LECS technology consists of an adder, registers and bus sellectors. The 1 chip 14 bit A/D and D/A converter LSI using LECS technology will be realized with 5μm CMOS LSI technology. Specifications as shown in Table 1 will be achieved using this high precision LSI.

Reference
(1) Kenji Maio et al. ISSCC digest, pp24-25, Feb., 1981.
(2) Ziya G. Beyacigiller et al. ISSCC digest, pp62-63, Feb., 1981.
(3) Y. S. Yee et al.,IEEE J. Solid-State Circuits, vol SC-14, pp778-781, Aug., 1979.

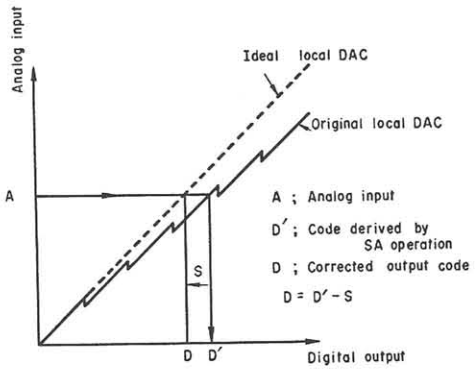

Fig. 1 LECS Technology Principle.

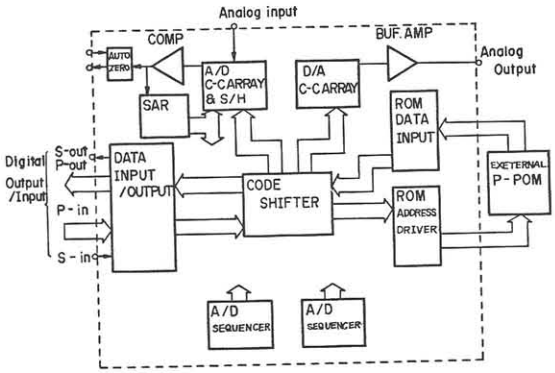

Fig. 4 1 chip A/D and D/A Converter LSI Blockdiagram using LECS Technology.

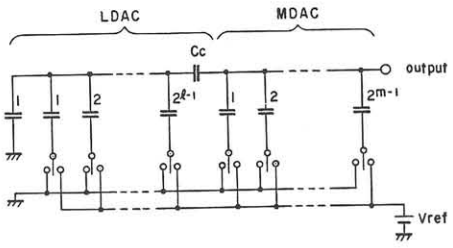

Fig. 2 Original DAC using C-C array

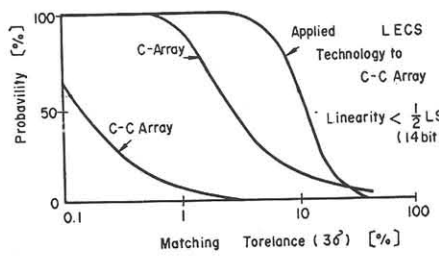

Fig. 3 Error Correction Effect Calculated Statistical Analysis.

Table 1. Specification for 1 chip A/D and D/A Converter LSI.

1chip A/D and D/A Converter LSI	Resolusion	> 14 bit
	Integral Linearity	< 1/2 LSB
	Maximum Sampling Frequency	50kHz 100kHz(A/D only) 150kHz(D/A only)
	Number of gate	1.8k gates
	Chip size	8 x 8 mm
Comparater	Cycle time (with C-Carray)	480 nS
	Delay from CLK	80 nS
Buffer Amplifier	Settling Time to 16 bit accuracy	< 1μS Load R=20kΩ C=50pF
	Linearity Error	< 1/4 LSB