A — 4 — 2 A 10 Bit All-Parallel A/D Converter

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Recently, 8 bit Monolithic A/D converters [1),2)] for digital processing of video signals were developed successively. However, 8 bit resolution is not sufficient for repeats of video signal dubbing or processing.

This paper will describe a monolithic all-parallel A/D converter with 10 bit resolution, 20 MHz conversion rate, performed with refined 3 μm bipolar process technology, using laser trimming polycrystalline silicon resistors. About 40,000 elements are integrated on a 9.2 x 9.8 mm^2 chip.

An all-parallel type A/D converter gives the best speed performance and needs no sample-and-hold circuit. However, there must be integrated 2^N-1 comparators which have high accuracy. Accordingly, for a 10 bit A/D converter, a full-scale range voltage of 2V, uncertainty of 1,023 comparators must be controlled to be less than 1 mV to realize 1/2 LSB accuracy.

A block diagram is shown in Figure 1. This converter contains 1,024 strobed comparators, encoding logics, clock drivers, output buffers, and adjustment circuitry for the dc reference voltages. Accuracy depends on the comparator offset due to the differential base-emitter voltages ΔV_{BE} between a transistor pair. ΔV_{BE} is affected mainly by h_{FE} differece which depends on emitter size.[2)] Figure 2 shows the dependence of ΔV_{BE} on emitter size. On the other hand, ΔV_{BE} of a pair transistor must be less than 0.5 mV in order to achieve 1/2 LSB accuracy. Therefore, the input transistor emitter sizes of the comparators are settled 12 μm square. Excepting the input transistors, standard size emitter and contact area are 6 x 6 μm^2 and 3 x 3 μm^2, respectively, and the value of f_T is 2 GHz.

In the all-parallel A/D converter, the accuracy also depends on the dc reference voltages, which are derived from single resistor line running through all the comparators in sequence. The linearity of the single resistor line made from aluminum is well within the 8 bit accuracy by itself. But the input current steered to 1,024 comparators causes the dc reference voltages nonlinear. To recover the nonlinearity, the adjustment circuitry which consists of operational amplifiers and laser trimmed polycrystalline silicon resistors is arranged. Sheet resistivity of the polycrystalline silicon is set to 300 Ω/□ having regard to the temperature coefficient.

Figure 3 shows linearity error and fractions of dc reference voltage versus output code number. Figure 4 shows a reconstructed linear ramp after sampling at

20 MHz conversion rate. Summary of typical characteristics is shown in Table 1. Figure 5 shows a photograph of 10 bit A/D converter chip.

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References

1) J.G. Peterson, IEEE J. Solid-State Circuits, SC-14, p.932 (1979)
2) T. Takemoto et al., Proceeding of the 13th Conference on Solid State Device, Tokyo, p.55 (1981)

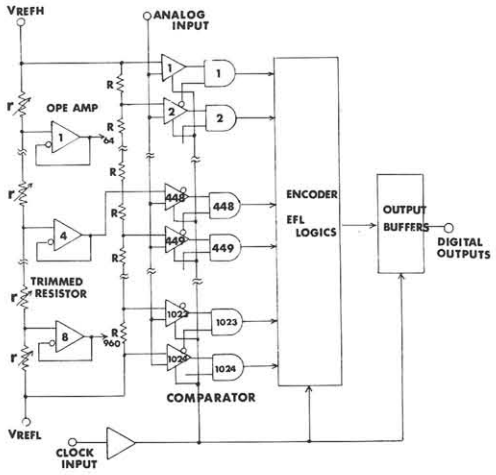

Fig.1 Block diagram of 10 bit A/D converter

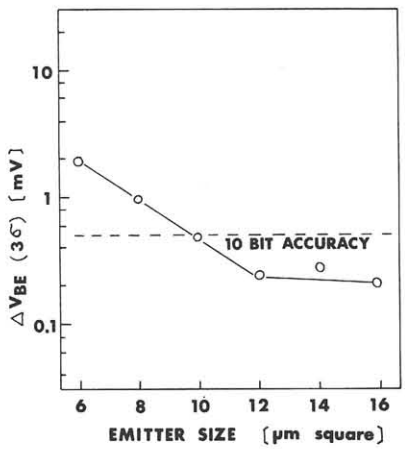

Fig.2 Dependence of ΔV_{BE} on emitter size.

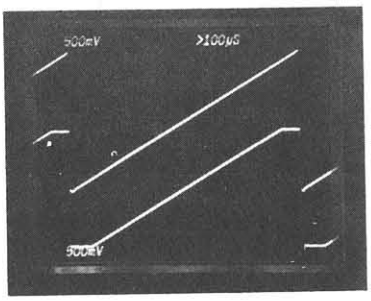

Fig.4 Original(top) and reconstracted(bottom) linear ramps at 20 MHz sampling rate.

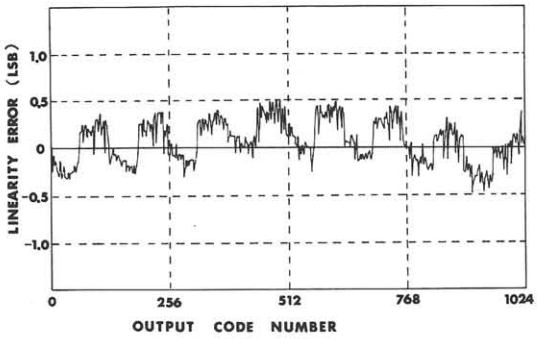

FIg.3 Plot of linearity error versus output code number.

Table 1 Summary of significant A/D characteristics.

A/D converter	
Resolution	10 Bit
Maximum conversion rate	20 MHz
Linearity	±1/2 LSB
Input voltage range	-2.0 V
Power	2.0 W
Number of devices	40,000
Chip size	9.2mm x 9.8mm
Transistor	
ΔV_{BE}	<0.5 mV
f_T	2 GHz

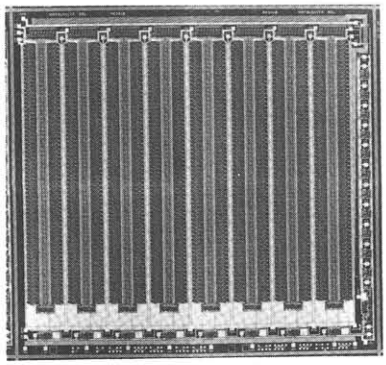

Fig.5 Photograph of 10 bit A/D converter chip.