

A-4-4 Very wide-band silicon bipolar monolithic amplifiers

M. Ohara T. Kamoto T. Sakai

Musashino Electrical Communication Laboratory, NTT

Musashino-shi, Tokyo, Japan.

Analog ICs, such as AGC and post amplifier, in the repeater circuits of a high speed optical fiber transmission system, were fabricated using an advanced silicon bipolar process technology called SST (Super Self aligned Process Technology)^{(1),(2)}. Good performance was obtained. This paper describes the design and performance for these analog ICs.

Figure 1 shows the configuration of the differential amplifier for a post amplifier. This circuit consists of a differential pair with emitter resistance, RE, and peaking capacitance, CP. This structure makes very wide band characteristics possible, because the feedback gain in the high frequency range is suppressed by peaking capacitance. Experimental frequency response is shown in Figure 2. The gain and 3dB down bandwidth are 15dB and 1.4 GHz, respectively. About twice the bandwidth for an ordinary differential amplifier is obtained.

Figure 3 shows an AGC amplifier configuration in which this peaking technology is applied. This circuit consists of two differential pairs with transistor, Q1, Q2 and Q3, Q4. The DC gain for each pair, Av1 and Av2, is

$$Av1 = R_c I_1 / (4V_T + 2(re + RE1)I_1), \quad Av2 = R_c I_2 / (4V_T + 2(re + RE2)I_2).$$
 Here VT is thermal voltage, and re is emitter resistance of the transistor. As load resistance, RL, is used commonly for these pairs, total DC gain, Av, is given by Av1+Av2. The gain control is effected by changing the ratio of I1 to I2 through a control voltage, Vc, in differential pair Q5, Q6. Accordingly, variable gain range, Avx, is given by $Av2(max) < Avx < Av1(max)$, where $RE2 > RE1$. The measured frequency response is given in Figure 4, along with the theoretical response predicted by computer simulation. The maximum gain and 3dB down bandwidth are 28dB and 630 MHz, respectively. A 30dB AGC dynamic range was obtained.

The features of this AGC amplifier are :

- (1). The DC current into RL is constant at all variable gain ranges, thus making it possible directly couple with the next amplifier stage without difficulty.
- (2). The Q3, Q4 pair, which has a larger emitter resistance, mainly operates, for large input signals, therefore, the linearity is excellent.
- (3). As an emitter peaking structure is used in Q1, Q2, which is the pair giving a higher gain, it is possible to double, or further expand the bandwidth in comparison with a non peaking structure.

For the purpose of realizing analog ICs, such as very wide band amplifiers, capacitors fabricated with an Al-Si₃N₄-Al structure were newly developed. This capacitor is free from voltage dependence and series resistance, and therefore, is suitable for use in a very wide band amplifier. Resistors were fabricated by boron doped polysilicon having a smaller parasitic capacitance.

Typical transistor parameters using these analog ICs are : emitter size, 1.7x10 μm², base resistance, R_b, 188Ω, collector to base capacitance, C_{cb}, 0.03PF, and the cut off frequency, f_T, about 7 GHz. In order to lower base resistance, which has an important effect upon frequency response, a double base electrode structure is used.

REFERENCES

- (1) T.Sakai et al., "A 3ns 1Kb RAM using Super Self Aligned Process Technology" in ISSCC Dig. Tech. Paper, pp.216-217, Feb. 1981.
- (2) T.Sakai et al., "High Speed Bipolar ICs Using Super Self-Aligned Process Technology" Proceedings of the 12th Conference on Solid State Devices, Tokyo, 1980.

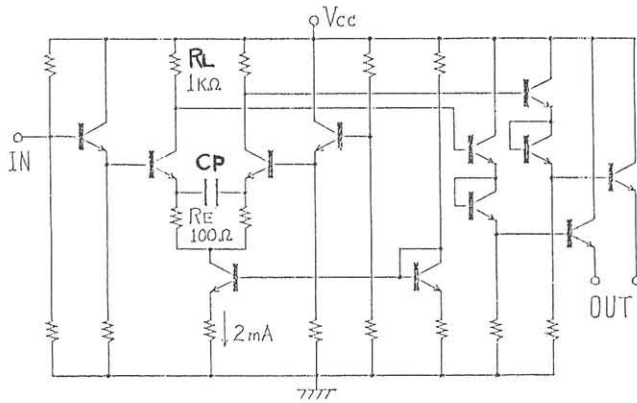


Fig. 1 Emitter-peaking differential amplifier.

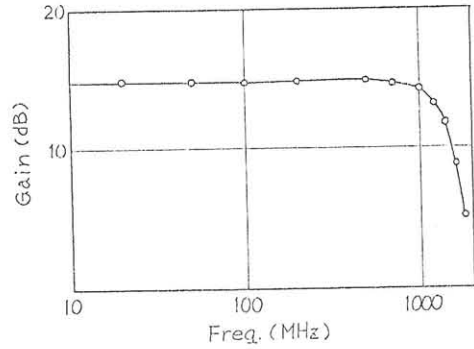


Fig. 2 Differential amplifier frequency response.

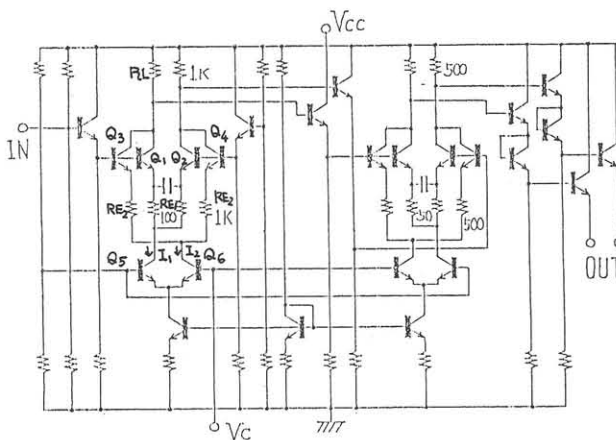


Fig. 3 Configuration of peaking type AGC amplifier.

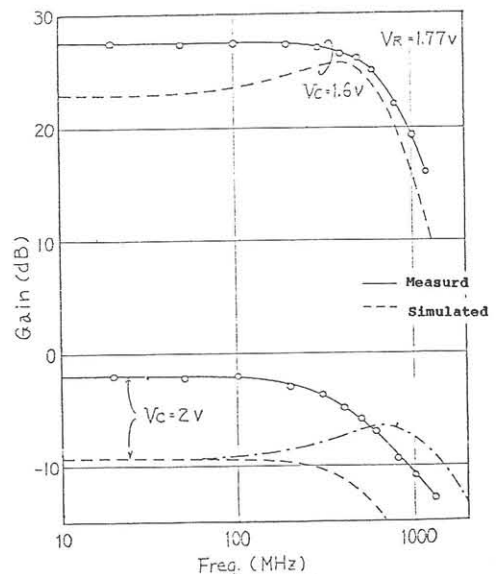


Fig. 4 AGC amplifier frequency response.