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A—4—5 A NEW HIGH POWER SWITCHING TRANSISTOR

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The overall objective of this paper is to present the development of device design and process techniques for the fabrication of high current, fast switching transistors in the range of 400-500 $V_{CEO(SUS)}$ range. This paper discusses how the results obtained on a 23mm device have been applied to a larger diameter (33mm) transistor. An improved base contact for equalizing the base-emitter voltage at high currents has been developed along with an improved emitter-contact preform which increases the silicon area available for current conduction. The electrical performance achieved is consistent with the theoretical optimum design. This paper describes the device design, water-processing techniques, and various measurements including forward SOA, DC characteristics and switching times.

Despite its age, the bipolar transistor is still one of the major switching components used for power electronics applications. For those cases where controlled turn-off is required, it is probably the dominant component. Presently, there are two important trends in the bipolar transistor industry. One trend is to increase the device area so that higher currents and voltages can be switched. The second trend involves improvements in characterization methods and understanding of the turn-off process. In this paper, we will present the fabrication and performance of a new experimental 33mm diameter transistor with a design of 500V, 150A with fast switching capability. A processing flow diagram indicating the various steps and the appropriate device cross section is shown in Figure 1. Most of the steps involved conventional silicon processing procedure with the exception being alloying, bevel grind, spin etch, and emitter preform attachment. For purposes of electrical testing, the emitter preform is held in place using a ring of RTV silicon elastomar. A photograph of the completed fusion element with the emitter contacting preform attached is shown in Figure II. The metallurgical emitter area for this design is $3.2cm^2$, and the emitter-base perimeter is 121cm. An example of the collector characteristic for a transistor of this design is shown in Figure III. The $V_{CEO(SUS)}$ for this transistor is 560V. The maximum gain current product is approximately 1400A at V_{CE} = 2.5V. Measured collector current fall-time in a clamped inductive turn-off circuit is approximately 0.2 μs for an I_C of 150A.

This paper shows how the results obtained on a 23mm device have been applied to a large diameter (33mm) transistor. Rather than simply scaling-up the previous

mask dimensions, a number of new ideas and modifications of the previous design have been made. These changes are:

1. An improved base-contact system for equalizing the base-emitter voltage at high currents.
2. An improved emitter-contact preform which increases the silicon area available for current conduction.
3. An increase in the amount of interdigitation of emitter and base, permitting one to achieve an h_{FE} vs I_C performance that more closely approximates the ideal case.

This paper will describe the design, processing, and measured electrical results of these new transistors.

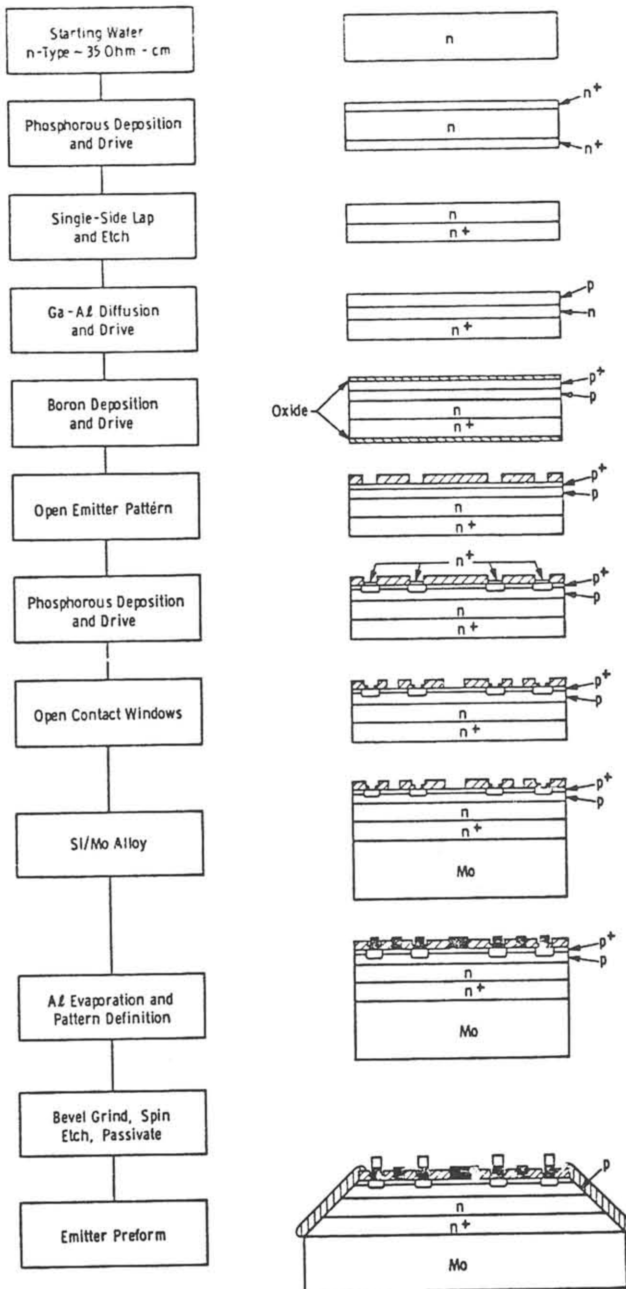

Figure I. Processing Flow Sheet with Device Cross Sections

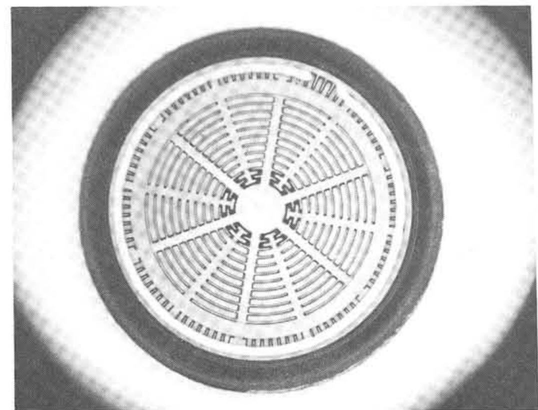

Figure II. Transistor Design Currently Under Development

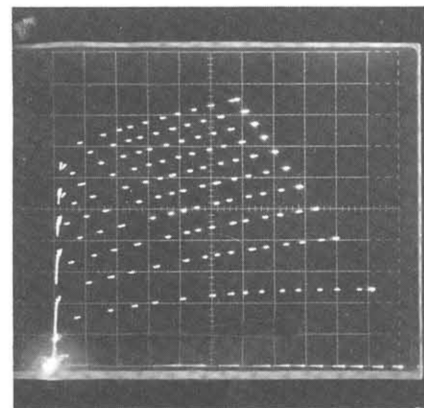

Figure III. Collector Characteristic for a Transistor.
Vertical: 50 A/d.
Horizontal: 1 V/d.
I_B = 10 A/step.