A — 4 — 6 Modeling of the "Bipolar mode" of operation of vertical JFET devices

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"Bipolar operation" of vertical JFET structures, such as SIT or FCT, is obtained if the gate is forward-biased with respect to the source. This is an attractive means to overcome the major drawbacks of FET devices, namely the relatively high on-resistance in saturation and the low current densities attainable, asking for large areas to obtain higher power devices.

Actually, very nice characteristics have been experimentally observed by many Authors[1,2,3] in bipolar mode vertical FET's, including low saturation voltage, high current gain and pentode-like output characteristics. However, there is a lack of exhaustive analysis of the device physics in that mode of operation, that could be applied to SIT's or power JFET's. In fact, if the spacing between the gates is not so small to have the channel completely depleted also in the forward-bias operation, the analysis developed in[4,5] cannot be applied.

The structure analyzed here, is the one displayed in Fig.1. It will be shown that closed-form solutions to the transport equations can be obtained in such a structure by splitting it into two quasi one-dimensional structures and by modeling the two regions with the help of the Regional Approximation Method. The results are able to accurately predict the performance of experimental devices and provide an insight in the physics of this operating mode of JFET's.

The analysis is performed by considering the $N^+N\,N^+$ (source-drain) and the $P^+N\,N^+$ (gate-source) structures separately and by accounting for the interrelationships between them. In the $N^+N\,N^+$ structure, we distinguish a conductivity-modulated Region, extending from the source transition and having a thickness, x_1, that is a function of bias voltages, and a drift region in which the non linear carrier velocity vs. field is accounted for. In the $P^+N\,N^+$ diode, the recombination in the highly-doped P^+ and N^+ regions is taken into account, together with a variable bulk recombination volume that is related to the thickness, x_1, of the conductivity-modulated region.

The model gives a detailed picture of carrier and field distributions both in the lateral channel direction (namely in the epilayer between the two gate P^+ regions) and in the vertical region (between source and drain). The model shows clearly the relevant role played by the minority-carriers injected by the gate regions, and the negligible value of the field within the conductivity-modulated region.

A first-order analytical model is also developed, based on the approximation of a linear carrier profile along the conductivity-modulated region and the assumption of ohmic conduction in the drift region of the epilayer. In the limits of that approximation, the saturation voltage can be written in terms of the gate, I_G, and drain, I_D, currents as:

$$V_{DS,sat} = 2V_T \ell n\{\left(\frac{I_G}{q(\alpha + qD_n \ell\, \alpha A_s/I_D)} + N_D\right)/\left(\frac{I_D W}{2qD_n A_s} + \left(\frac{I_G}{q(\alpha + qD_n \ell\, \alpha A_s/I_D)}\right)^{\frac{1}{2}} + N_D\right)\} \quad (1)$$

where $\alpha=(A_s D_{ps}/W_s N_{Ds})+(A_g D_{ng}/L_{ng} N_{Ag})$ is a parameter that accounts for the recombination in the gate and source highly-doped regions, ℓ is the length of the stripe, A_s is the source area, the other symbols are defined in Fig.1. In the active region the I_D-V_{DS} curves are expressed as:

$$I_G = \frac{q N_D^2}{4 V_T^2} (\alpha + \frac{qD_n \ell a A_s}{\tau N_D}) (\frac{W I_D}{\sigma A_s} - V_{DS})^2 \qquad (2)$$

where σ is the epilayer conductivity, τ is the epilayer lifetime.

The small-signal current gain, h_{fe}, can be obtained from Eq.2 as:

$$h_{fe} = \frac{4qD_n^2 A_s^2}{W^2} \{ 2\alpha I_D (1 - \frac{V_{DS}\sigma A_s}{I_D W}) + \frac{qD_n \ell a A_s}{\tau} (1 - (\frac{V_{DS}\sigma A_s}{I_D W})^2 \}^{-1} \qquad (3)$$

In Fig.2,3 there are reported, as an example, the theoretical results obtained by using Eq.1,2,3 (solid lines) and the experimental results measured on an interdigitated structure, similar to the one reported in Fig.1. On the basis of those plots, the effects of the main design parameters on the device behavior are discussed and justified by using the physical model proposed.

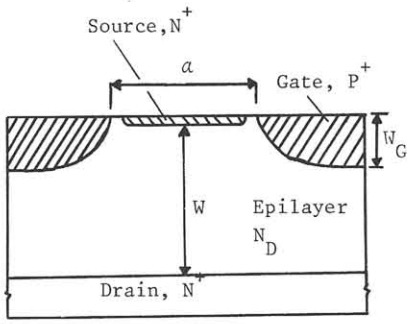

Fig.1 Structure of the device.

References

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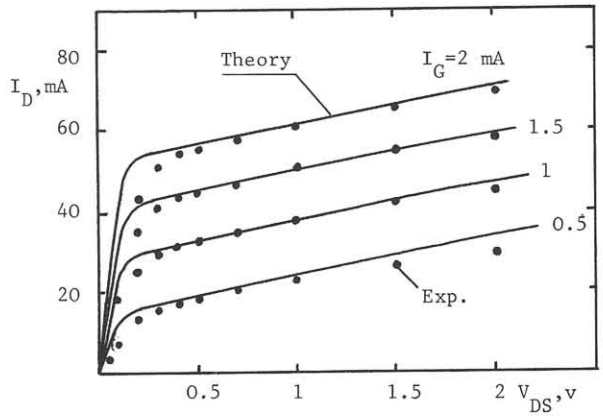

Fig.2 Output characteristics of bipolar mode vertical JFET.

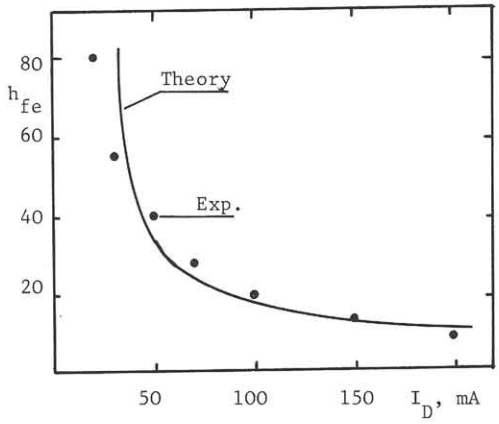

Fig.3 Small-signal current gain.