

A-4-8 Precision Reactive Etching & Its Applications

J. S. Lechaton, G. Srinivasan, S. Gaur

IBM General Technology Division, East Fishkill

Hopewell Junction, New York 12533, U.S.A.

Anisotropic reactive sputter etching (RSE) is used extensively for forming high-resolution patterns in semiconductor materials. While this property is very useful for increasing device density, a new application - precision etching - is emerging which shows much promise for modifying silicon device characteristics and for creating new device structures. In addition, this technique prevents mask undercutting that is associated with wet etching. Reactive etching with the proper in situ etch depth monitor can be used to etch to precise depths within a few hundred angstroms. This paper presents the method for controlling this depth and experimental results which demonstrate the application of precision RSE to modify device structures. The tool we used for this type of etching has been described elsewhere<sup>1</sup>. Briefly, the wafers to be etched are placed on a fused silica product plate ( $\sim 18$ cm diameter) which is bonded to a water cooled electrode. The r.f. power (13.56 MHz) is applied to the substrate electrode. Typical operating conditions are 40 watts ( $0.16 \text{ w/cm}^2$ ), 10mTorr and 10 sccm of  $\text{Cl}_2/\text{Ar}$ . The percent  $\text{Cl}_2$  is varied from 3% to 7% to control the etch rate which is influenced by the silicon loading.

The key to precision etching is in in situ monitoring of the etch depth. The optical interference from a polysilicon film on a thermal oxide wafer is excellent for this purpose. Because the index of refraction of polysilicon is high ( $\sim 3.73$ ), the amount of silicon removed per interference fringe, at normal incidence of a helium-neon laser ( $6328\text{\AA}$ ), is 85.0nm. By etching half integrals of a fringe, it is possible to remove silicon in increments of  $\sim 43$ nm with a total error in depth of  $< \pm 10$ nm. For our applications, the index was determined for several boron concentrations in a CVD polysilicon film by etching an integral number of fringes and measuring the step with a Sloan Dektak. The index was determined from the equation:  $n = N\lambda/2d$ . Our results indicate that the index ( $\sim 3.78$ ) did not vary significantly with boron concentrations<sup>2</sup>. The polysilicon film is used as an in situ etch monitor for etching devices in single crystal silicon after an initial calibration with Dektak measurements. The calibration showed that the boron doped ( $\sim 4 \times 10^{18}/\text{cm}^3$ ) single crystal wafer etched  $\sim 6\%$  slower than polysilicon films, so that one fringe from the polysilicon monitor corresponds to  $\sim 80$ nm in the single crystal wafer.

This precision etching has been used for several applications. We have

reduced the intrinsic base width in increments of 40nm by RSE removal of part of the defused base prior to the emitter diffusion. The electrical characteristics of these devices will be reported later this year<sup>3</sup>. The uniformity and repeatability of etching were determined by measuring the current gain ( $\beta$ ) on devices fabricated in a 82-mm diameter wafer in which the base was etched by 80nm with two wafers at a time and in four runs. Measurements showed that the  $\beta$  variation in  $\beta$  was less than 14%. It was also found the  $\beta$  was slightly higher at the wafer perimeter than at the center, which may be due to a high etch rate at the wafer edge. The precision etching was also used to study the effect of emitter depth on current gain. The  $\beta$  decreases significantly for an emitter depth below 200nm because of enhanced hole diffusion<sup>4</sup>. However, barrier layers such as Cr-CrOx did not further degrade these shallow emitter devices.

Two of the concerns of RSE applications are the contamination from non-volatile reaction products and crystal damage to the device surface from ion bombardment. We have found that etching the device surface at low powers ( 0.16 watts/cm<sup>2</sup>), particularly in Cl<sub>2</sub>/Ar, did not noticeably degrade the device. The device yield after thinning the base by 800Å (99.8%) compares favorably with unetched devices (99-100%). The emitter-base breakdown voltage remained unchanged at 4.5V at 20μA after base etching. This is consistent with a recent report on the removal of surface damage by Cl<sub>2</sub>/Ar etching after CF<sub>4</sub>/H<sub>2</sub> etching<sup>5</sup>.

RSE can also be used as a precision etching tool to modify device characteristics selectively on a chip. We have demonstrated that the process is repeatable with acceptable uniformity across the wafer and that there is no device degradation when etched with Cl<sub>2</sub>/Ar at low powers. We believe that this technique will become increasingly important in the future for making new device structures.

#### REFERENCES

- 1: J. S. Lechaton, J. L. Mauer, Proc. of the Symposium on Plasma Etching & Deposition 81-1 75 (1981) ECS.
- 2: These results are consistent with an independent measurement of  $n=3.73$  for undoped poly-Si by W. A. Pliskin, IBM East Fishkill-Private Comm.
- 3: G. Srinivasan et. al. Base Etched Transistor, to be published.
- 4: S. P. Gaur, G. R. Srinivasan & I. Antipov, IEDM, pg. 276, 1980
- 5: Y. Horiike et. al. Jpn. J/APPL Physc 20, 803 (1981) #4

#### ACKNOWLEDGEMENTS

The authors thank C. MacPherson and R. Gray for their assistance in Reactive Etching.